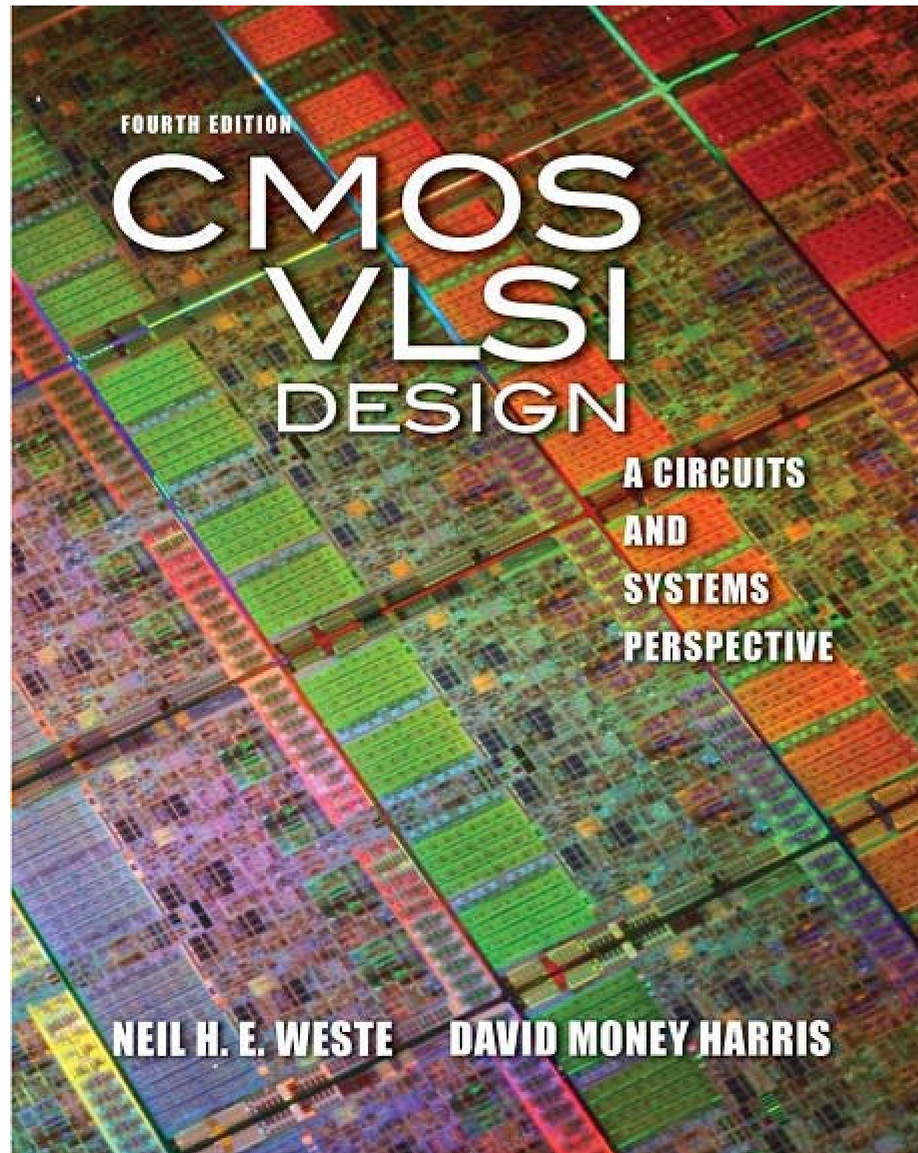


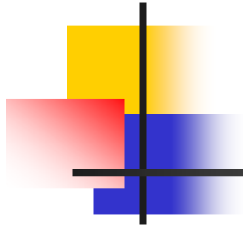
Lecture 0: Introduction

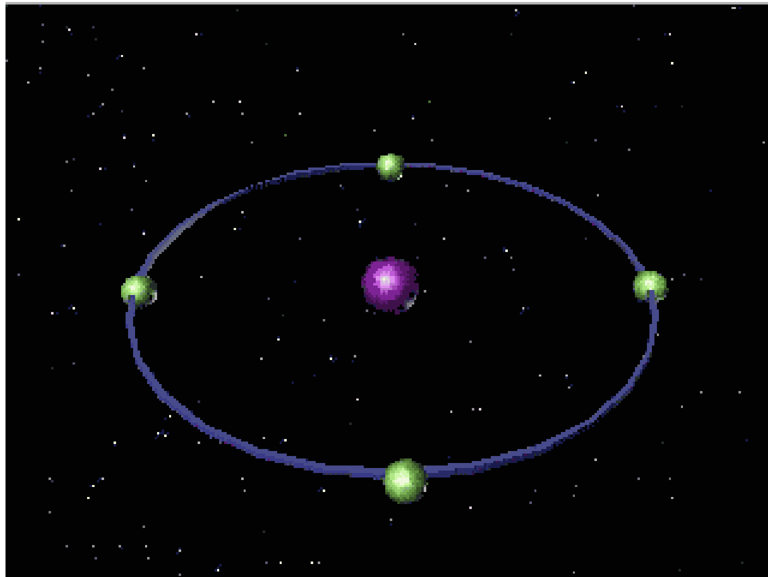
Introduction

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): bucketloads!
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- Today: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

矽的簡介

矽是現在各種半導體中使用最廣泛的電子材料，它的來源極廣，譬如我們腳下所踩的砂。它的含量佔地球表層的25%，純化製作容易，取得成本較低，因此被用來做為積體電路 製作的主要材料。如常見的微處理器（CPU)，動態隨機存取記憶體（DRAM）、、、等，皆是以矽為主要材料。在元素週期表裡，它是屬於四價元素，排在三價的鋁與五價的磷之間。



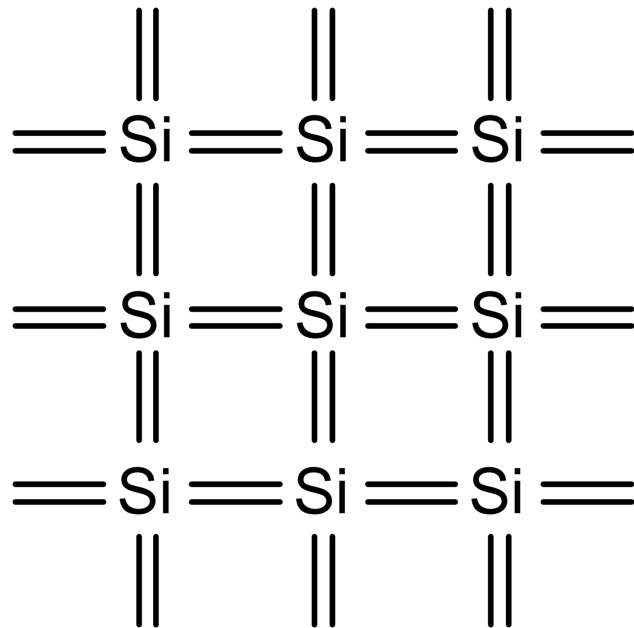


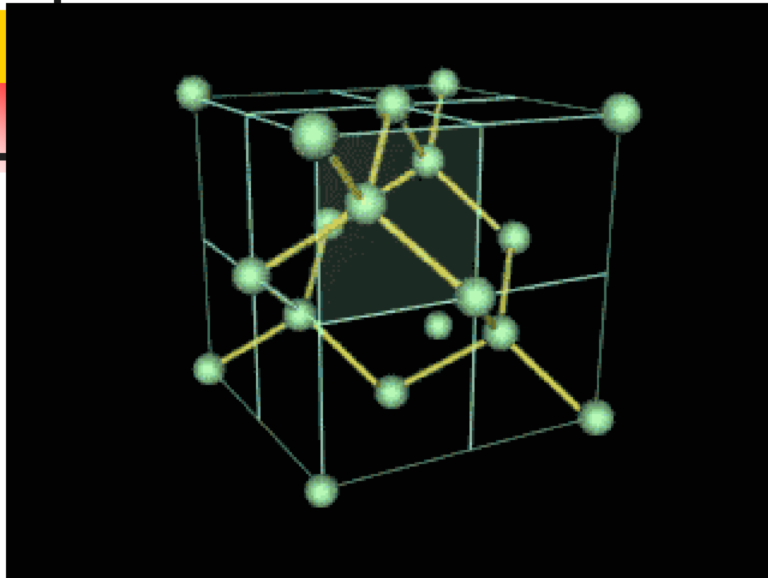
矽原子與電子圖

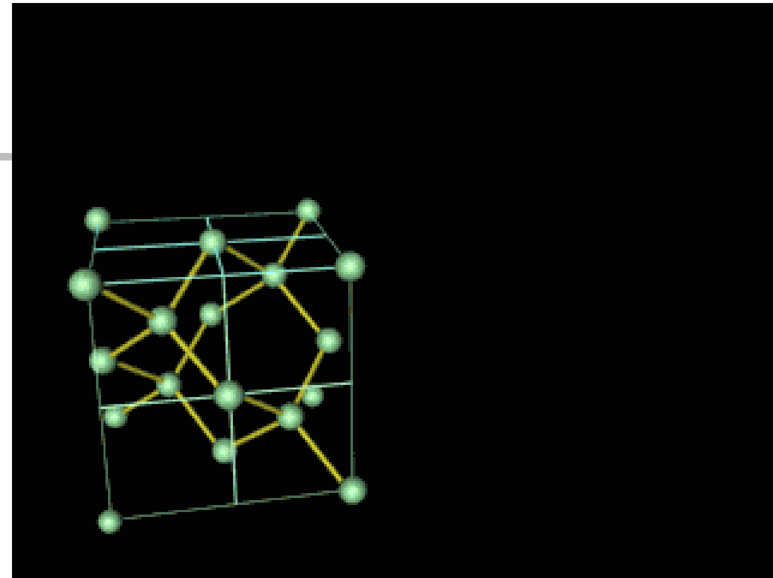
矽是屬於四價元素，原子序為14，雖然原子內所含的電子相當多，但是因為較接近原子核的電子被外層電子所遮蔽，所以內層電子對整體材料的電性影響也比較小，我們將探討矽原子的4個外圍電子，也就是價電子。

Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors







鑽石結構

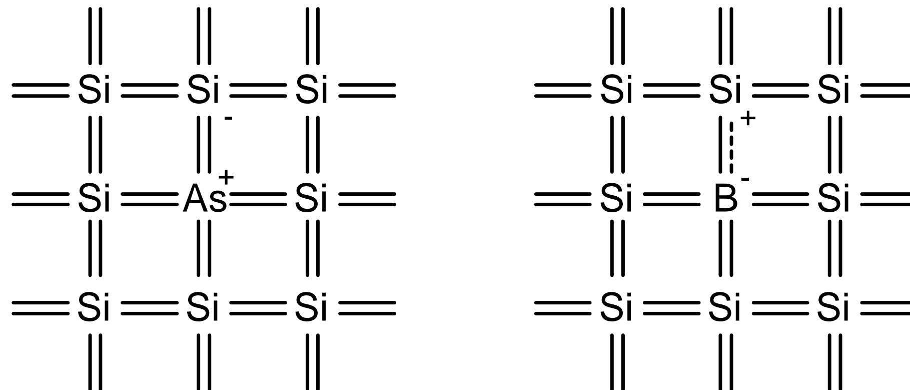
在三度空間中，矽晶體由許許多多四面體單元連結構成，四面體中心有一個矽原子，此外有四個矽原子位在四面體上的四個端點，八個四面體構成的立方結構稱為鑽石結構。

矽的結構

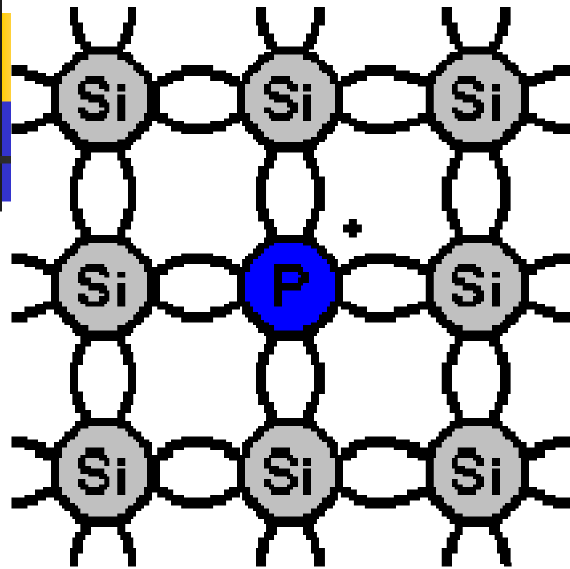
矽晶體便是以鑽石結構為單位，晶體內的矽原子在三度空間中，以週期性方式排列。

Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)

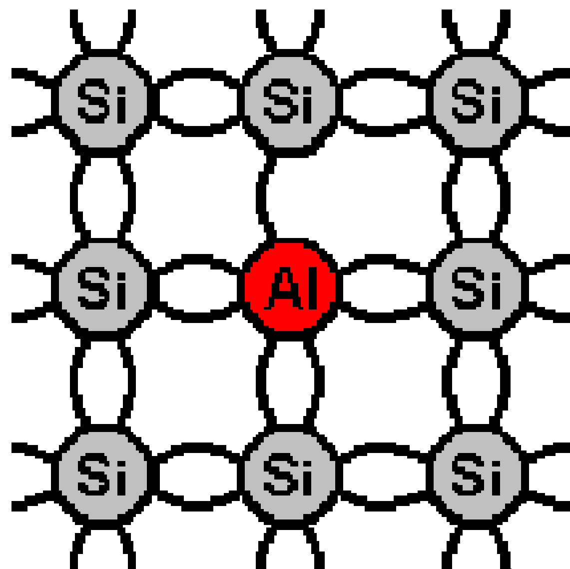


摻 雜 (Doping)



負摻雜

在矽晶體中，摻入週期表中的五族元素（此摻入的五族元素稱為施體）。由於要和矽鍵結需要四個電子，五族元素原子卻可提供五個電子，摻雜原子多出了一個電子，當外加一個電壓時，電子向正電位處移動，形成了電的傳導。此摻雜的區域即稱為負型區(n-type region)，主要的傳導載子(carrier)為電子。

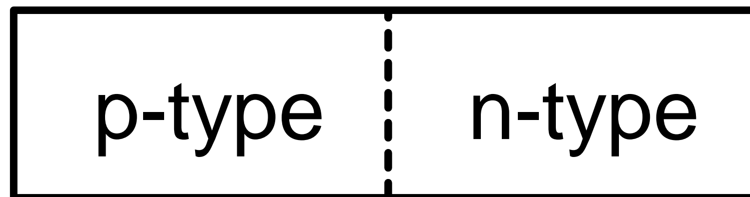


正摻雜

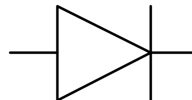
在矽晶體中，摻入週期表中的三族元素（此摻入的三族元素稱為受體），由於和矽原子鍵結需要四個電子，三族元素原子僅可供應三個電子，因而形成了一個電子的空缺，我們稱之為電洞。當外加一個電壓時，電洞向負電位處移動，形成了電的傳導。此摻雜的區域即稱為正型區(p-type region)，主要的傳導載子(carrier)為電洞。

p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

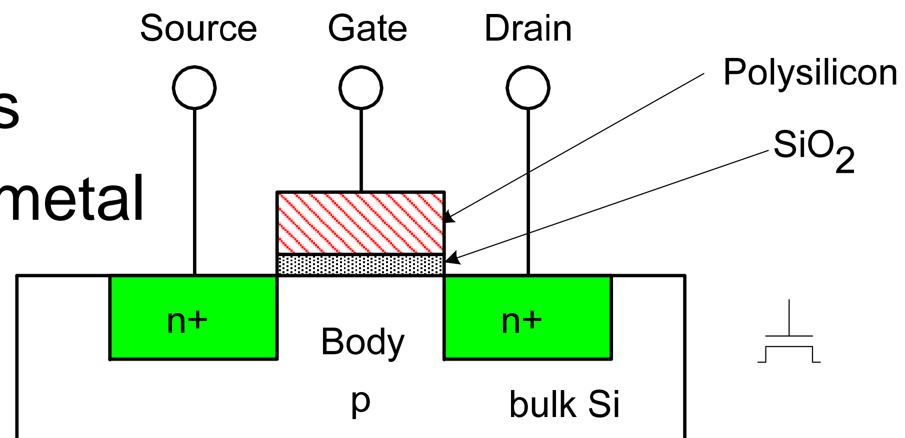


anode cathode



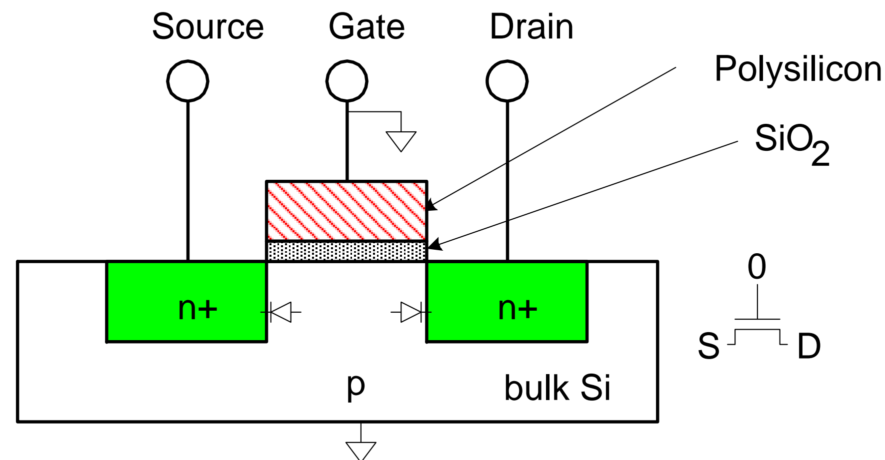
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



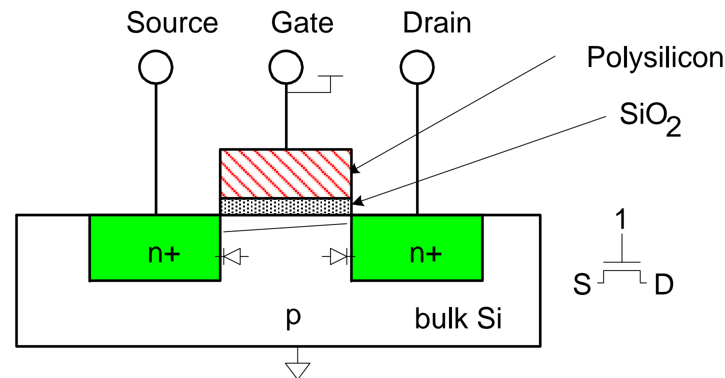
nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



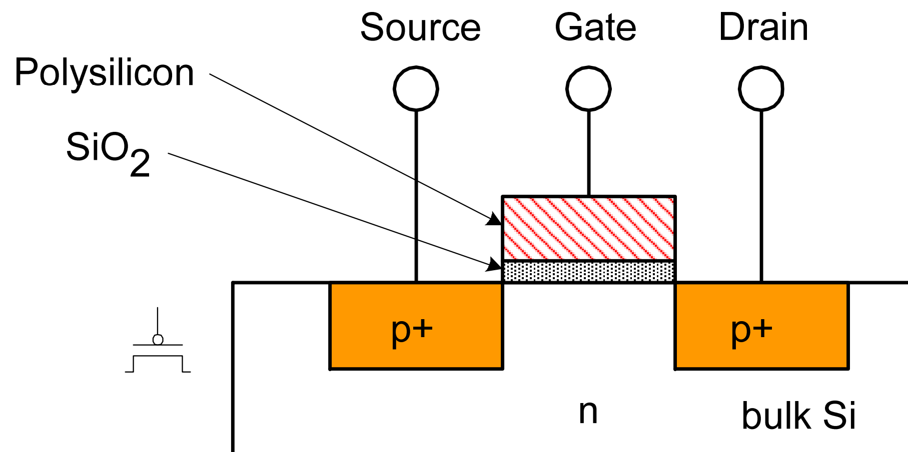
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

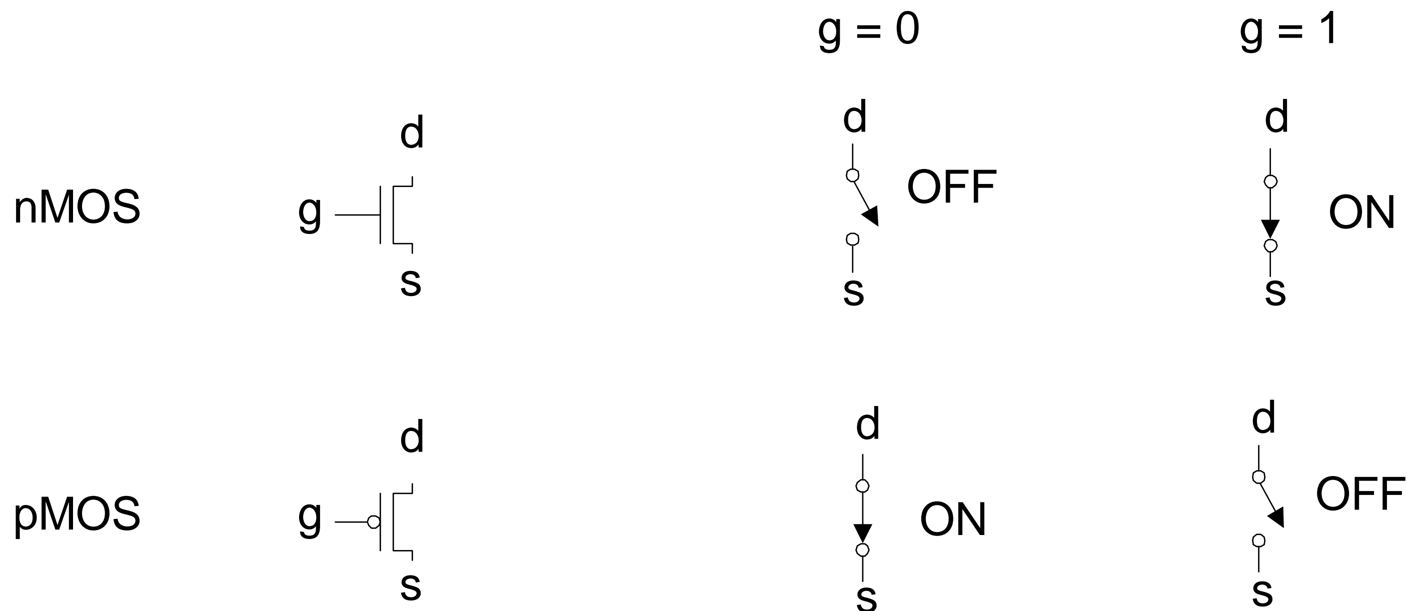


Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

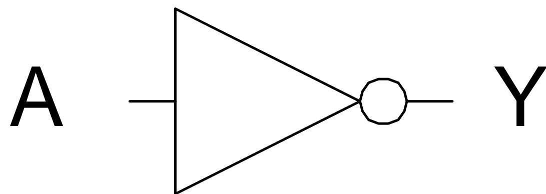
Transistors as Switches

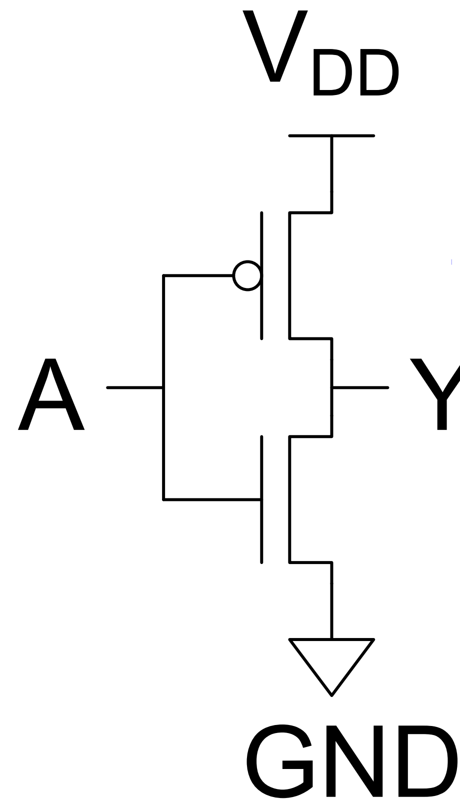
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

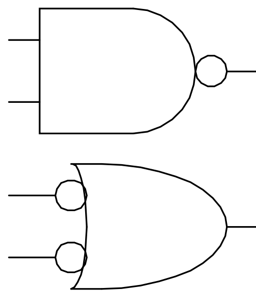
A	Y

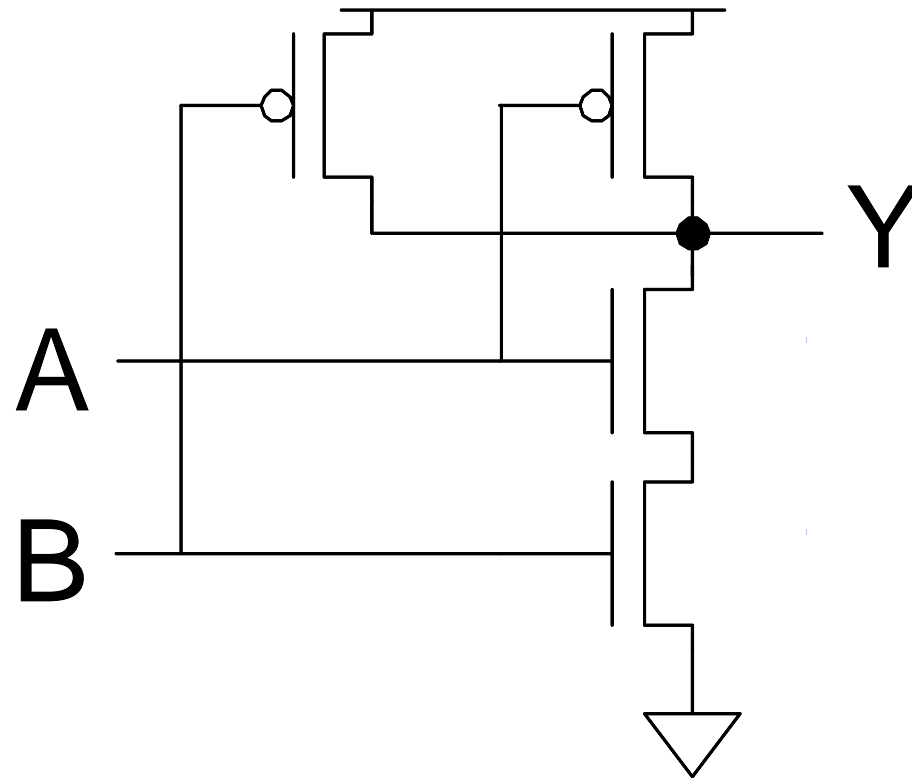




CMOS NAND Gate

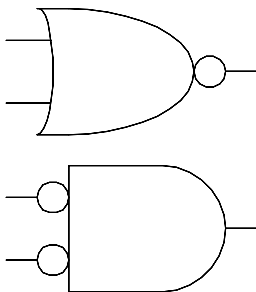
A	B	Y
0	0	
0	1	
1	0	
1	1	

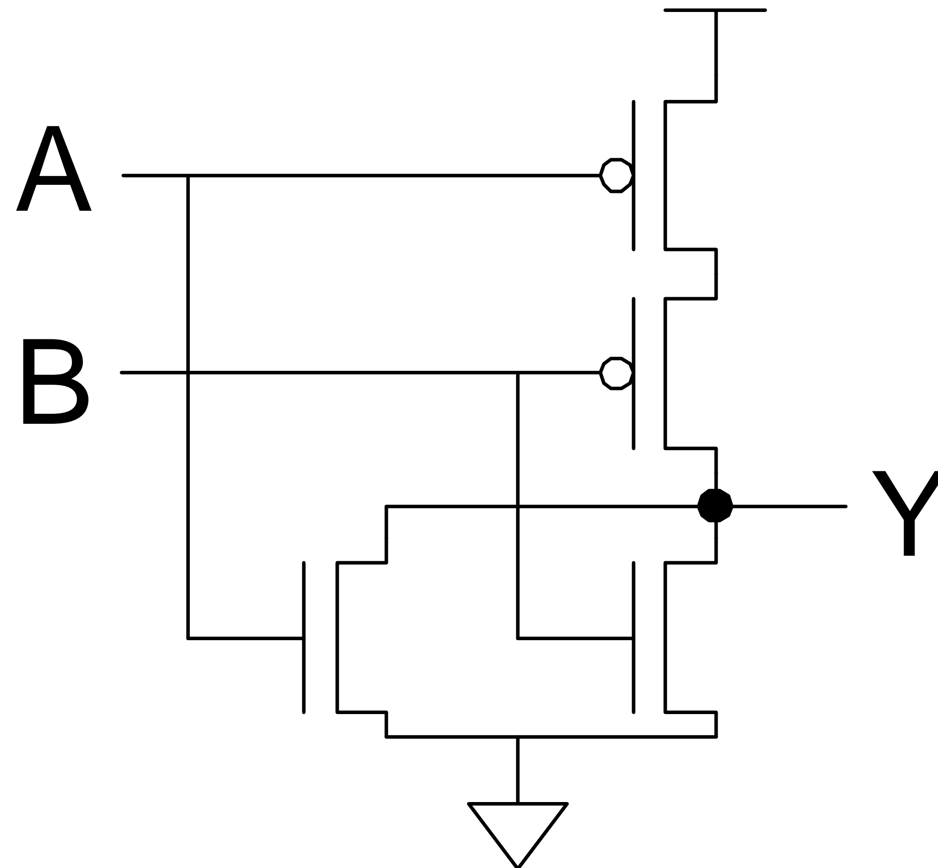




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





3-input NAND Gate

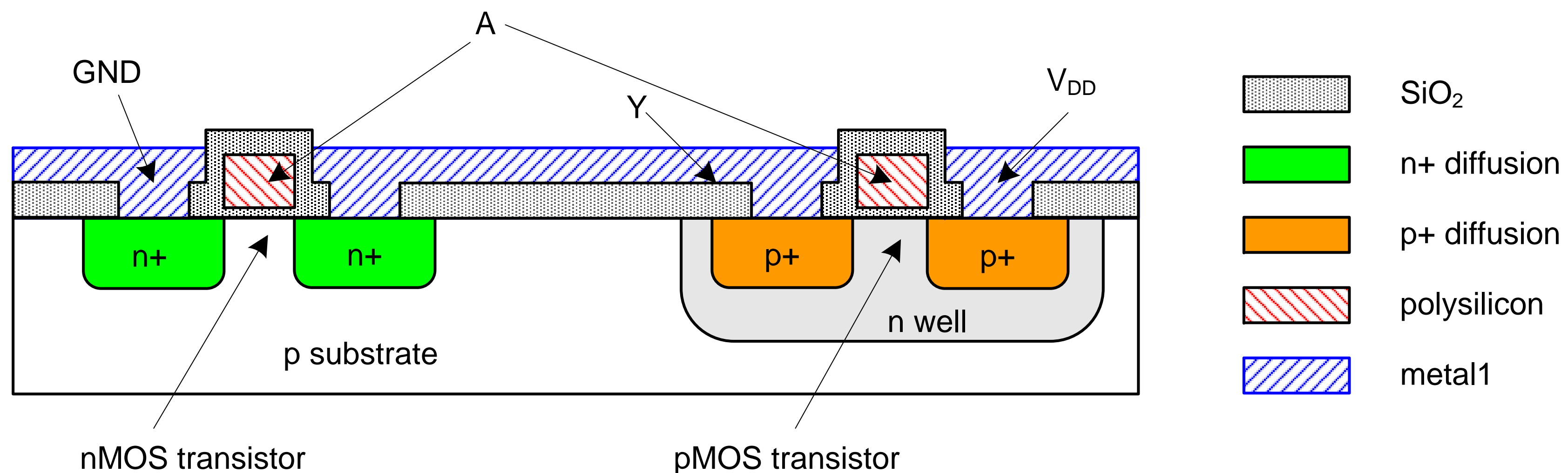
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

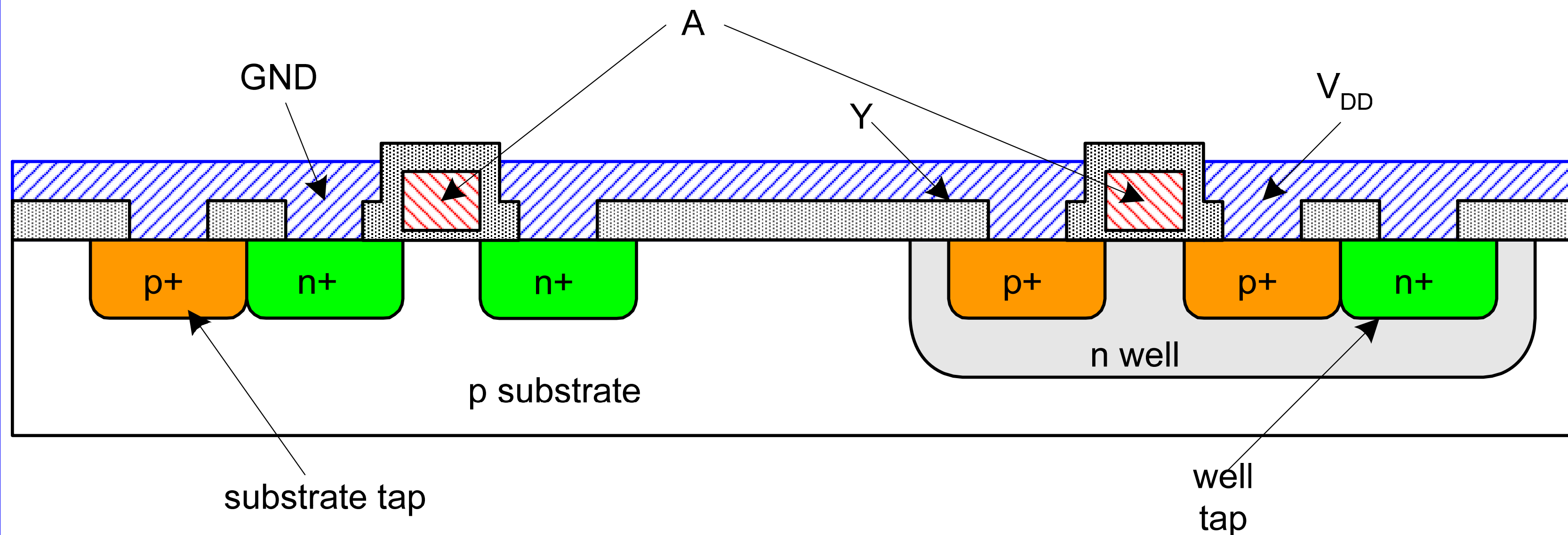
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



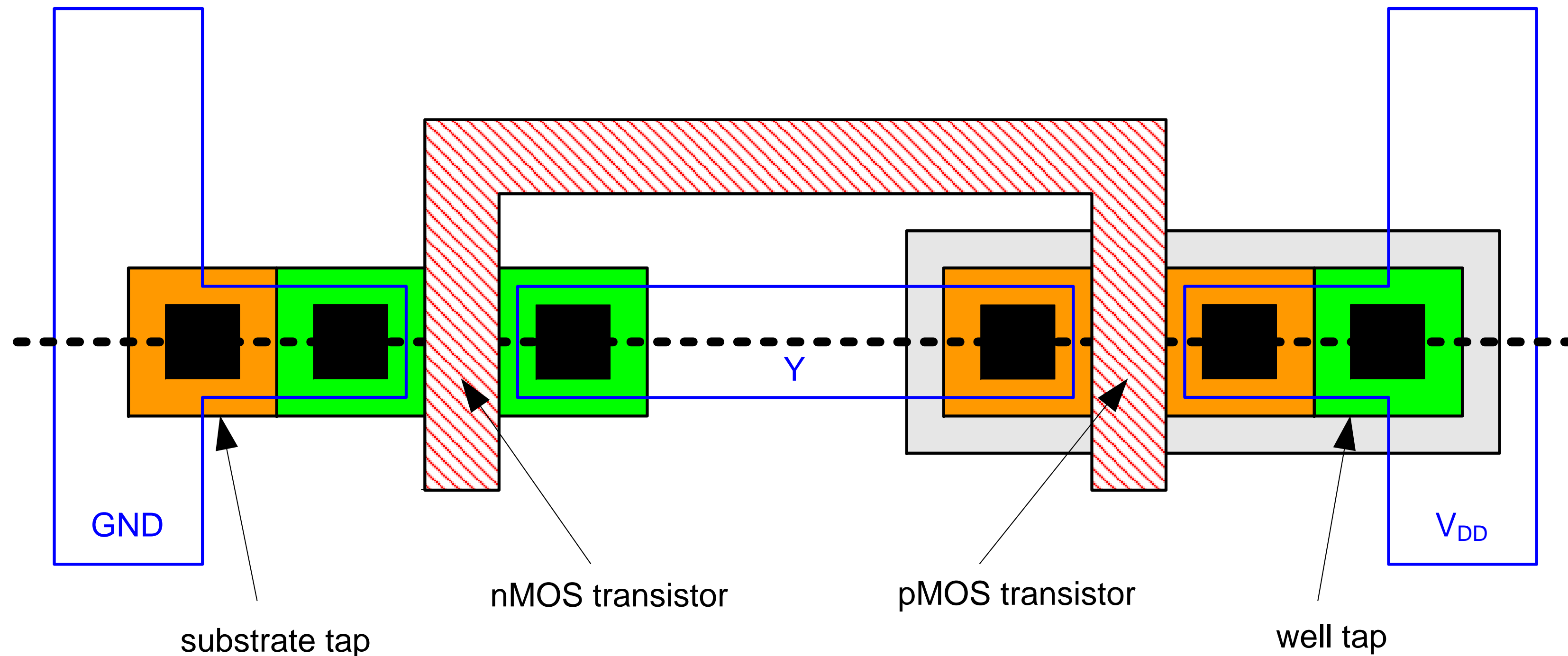
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



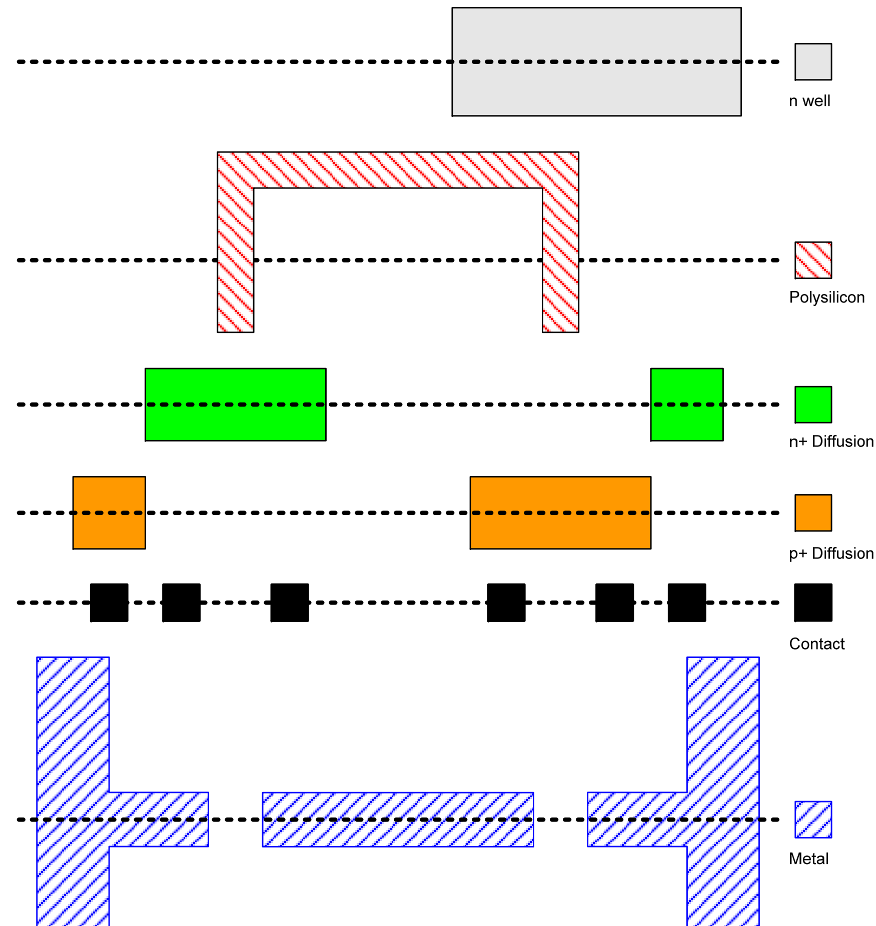
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



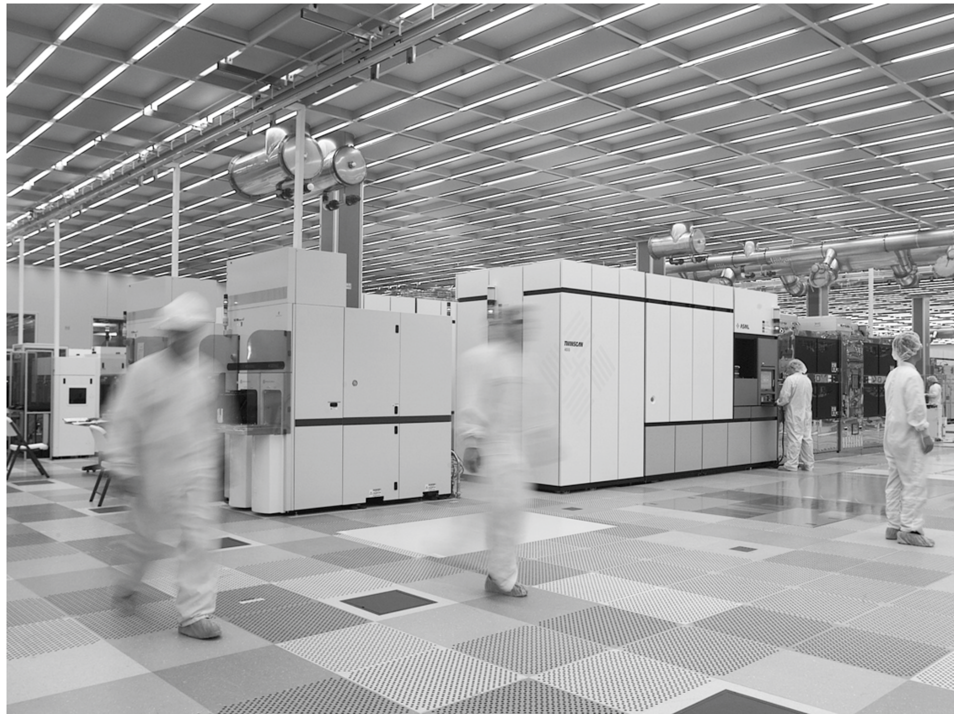
Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal



Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields



Courtesy of International
Business Machines Corporation.
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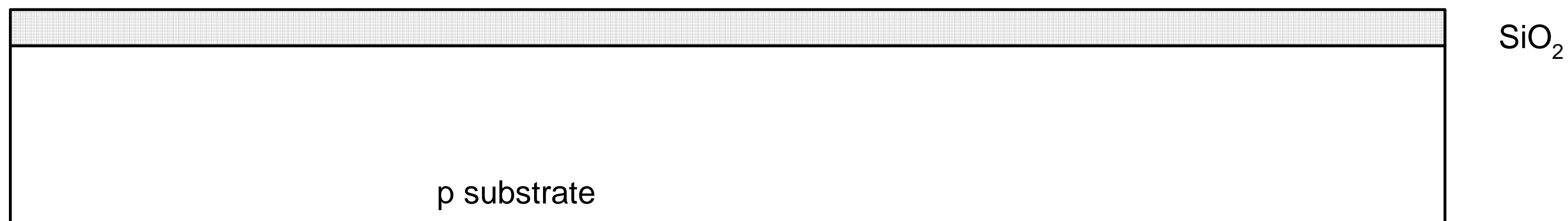
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

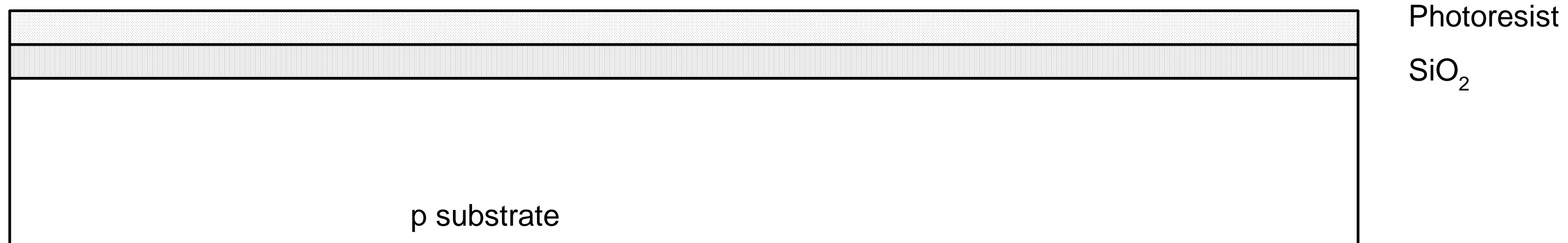
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



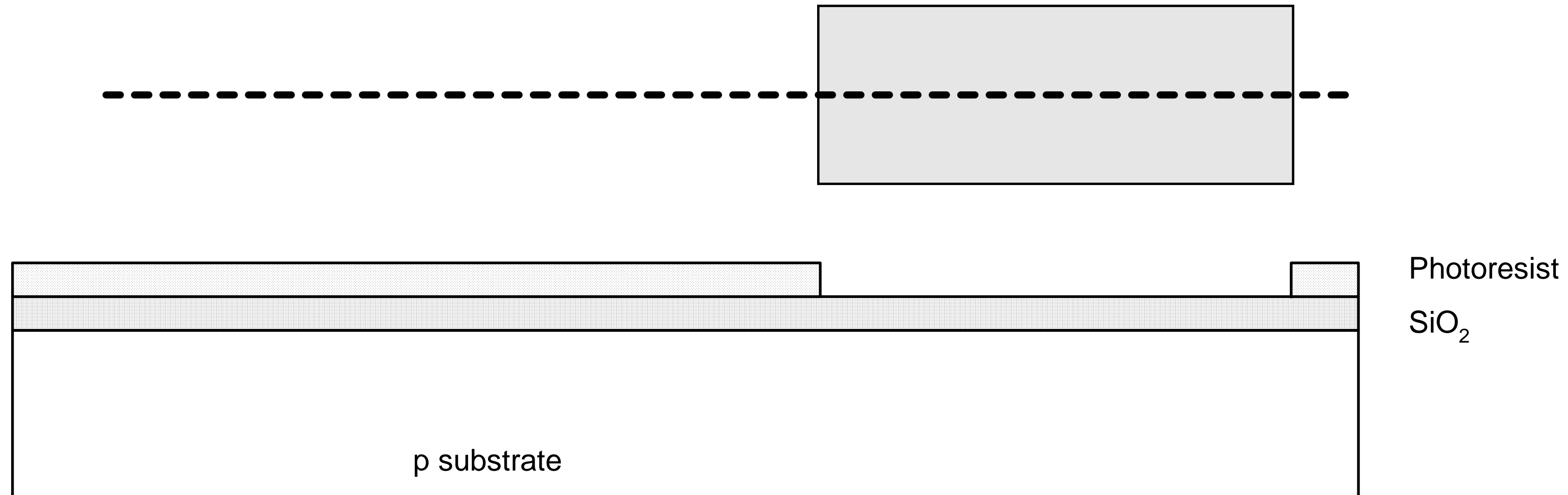
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



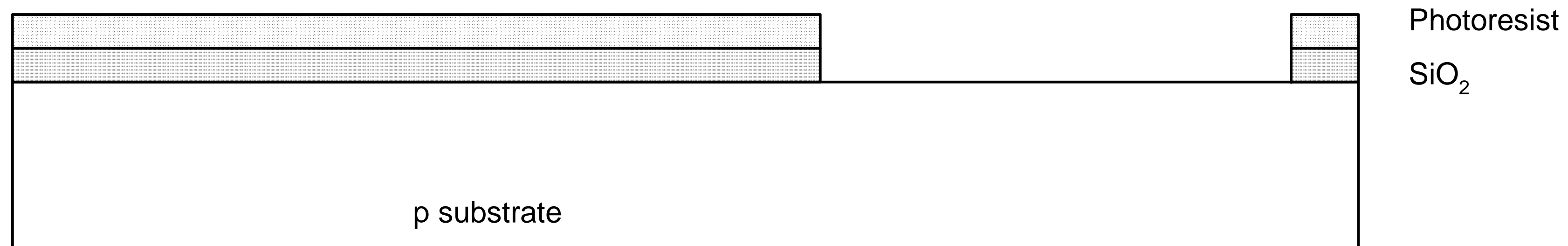
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



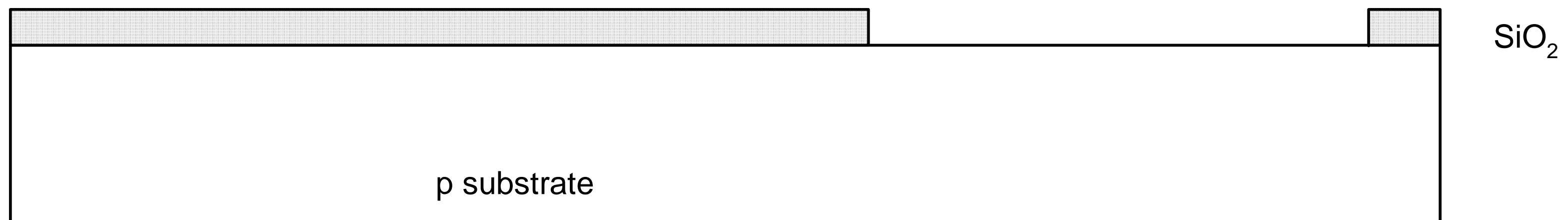
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



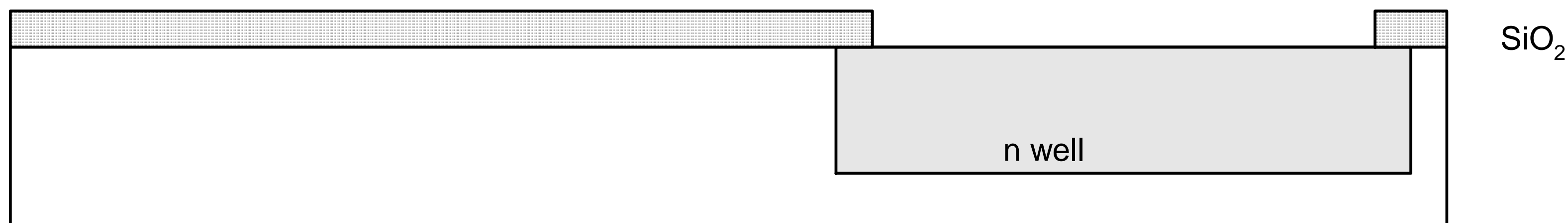
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranha etch
- Necessary so resist doesn't melt in next step



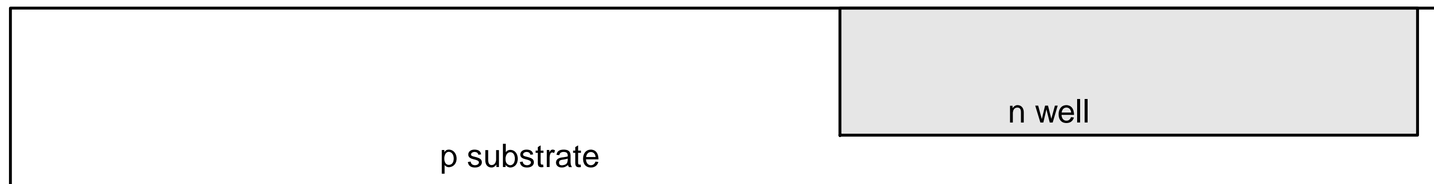
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  – Place wafer in furnace with arsenic gas
  – Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  – Blast wafer with beam of As ions
  – Ions blocked by SiO_2, only enter exposed Si



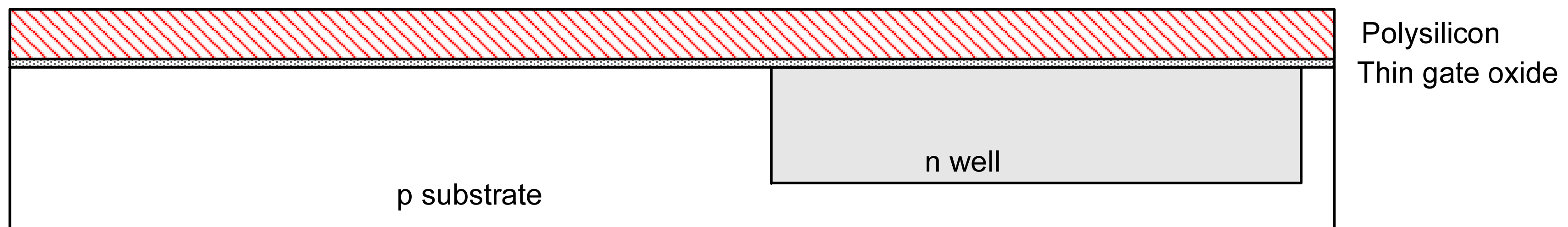
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



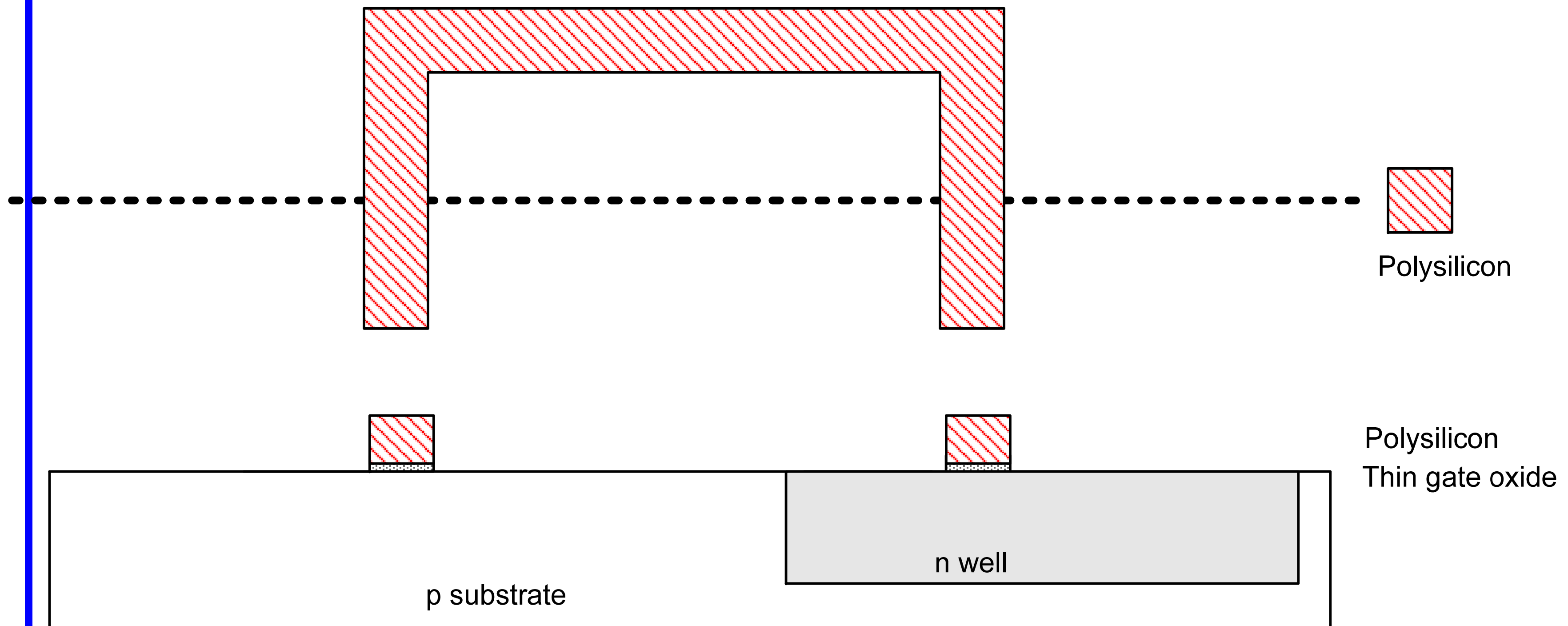
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



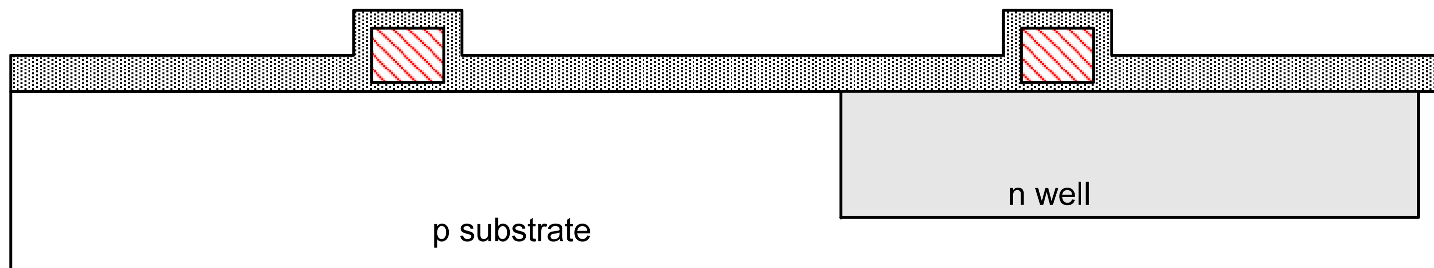
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



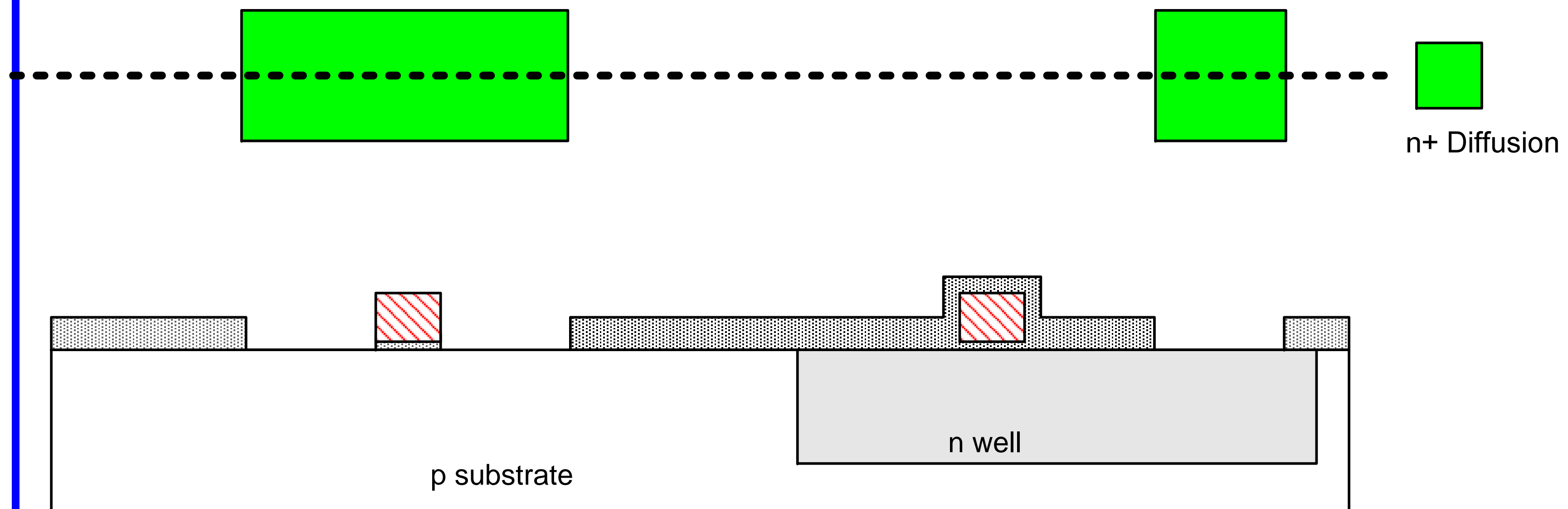
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



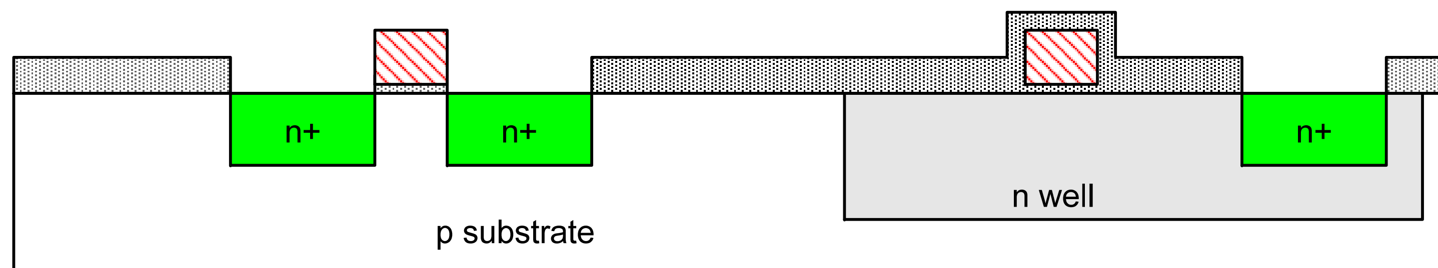
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



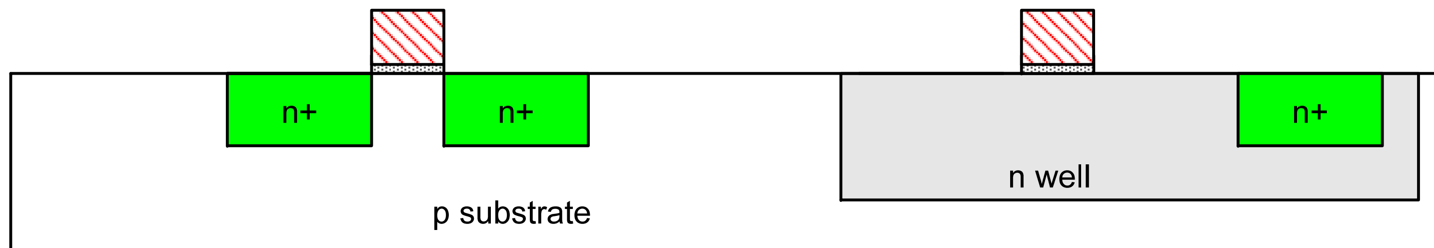
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



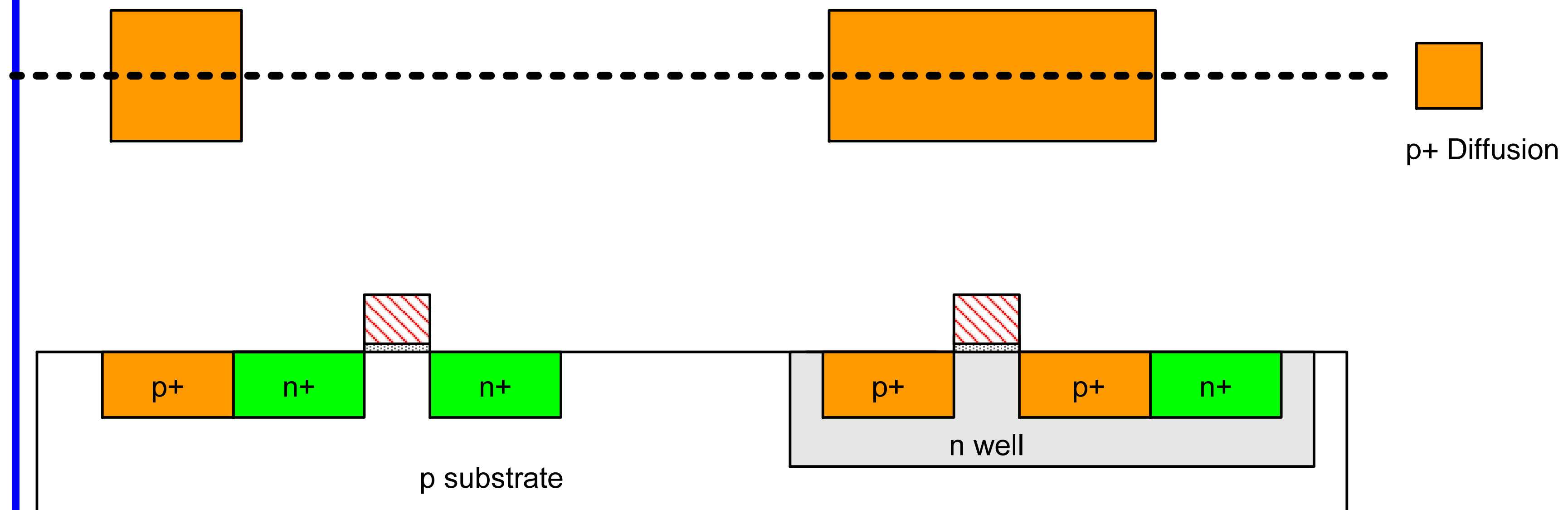
N-diffusion cont.

- Strip off oxide to complete patterning step



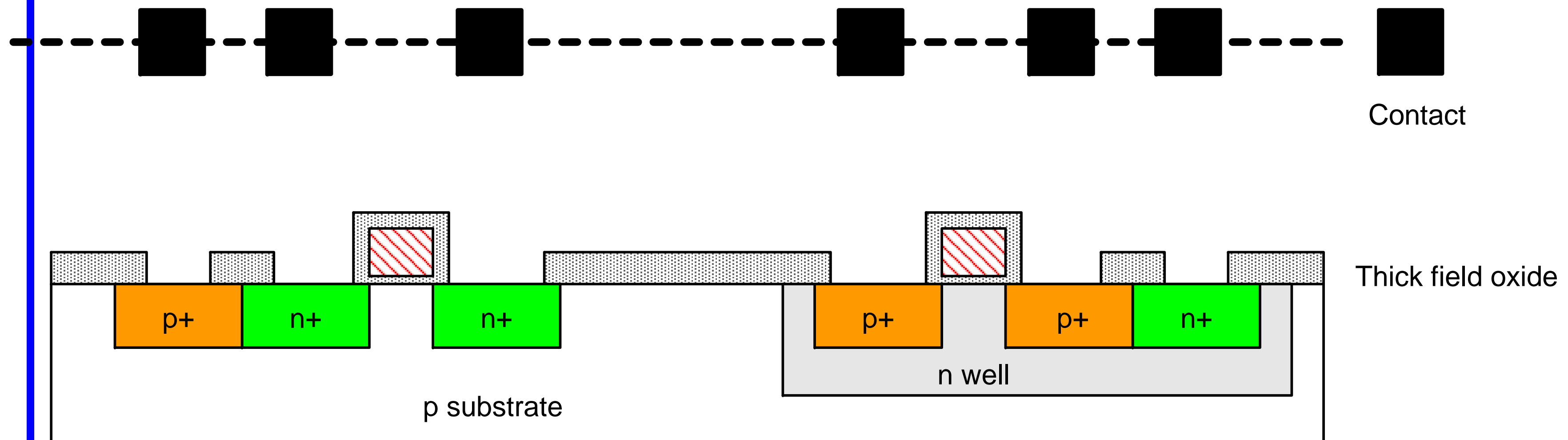
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



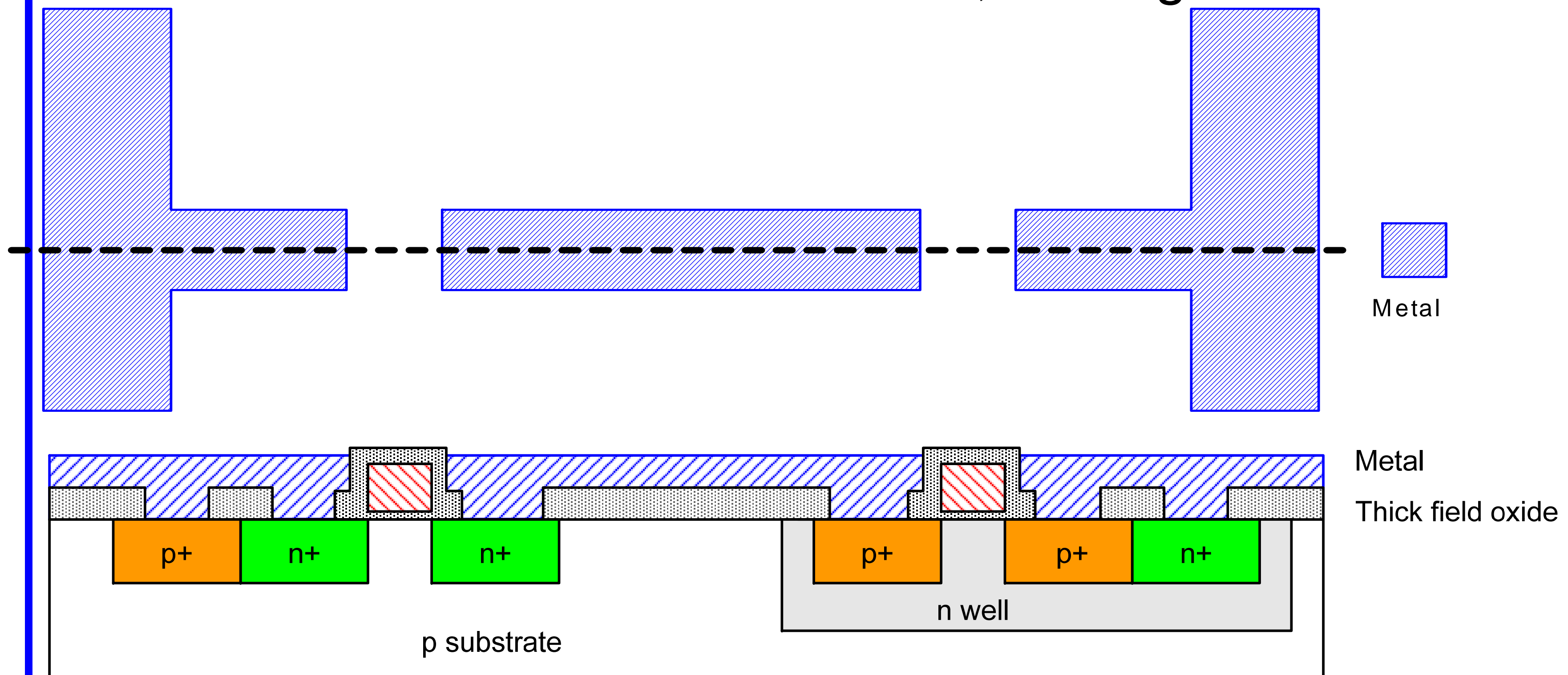
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

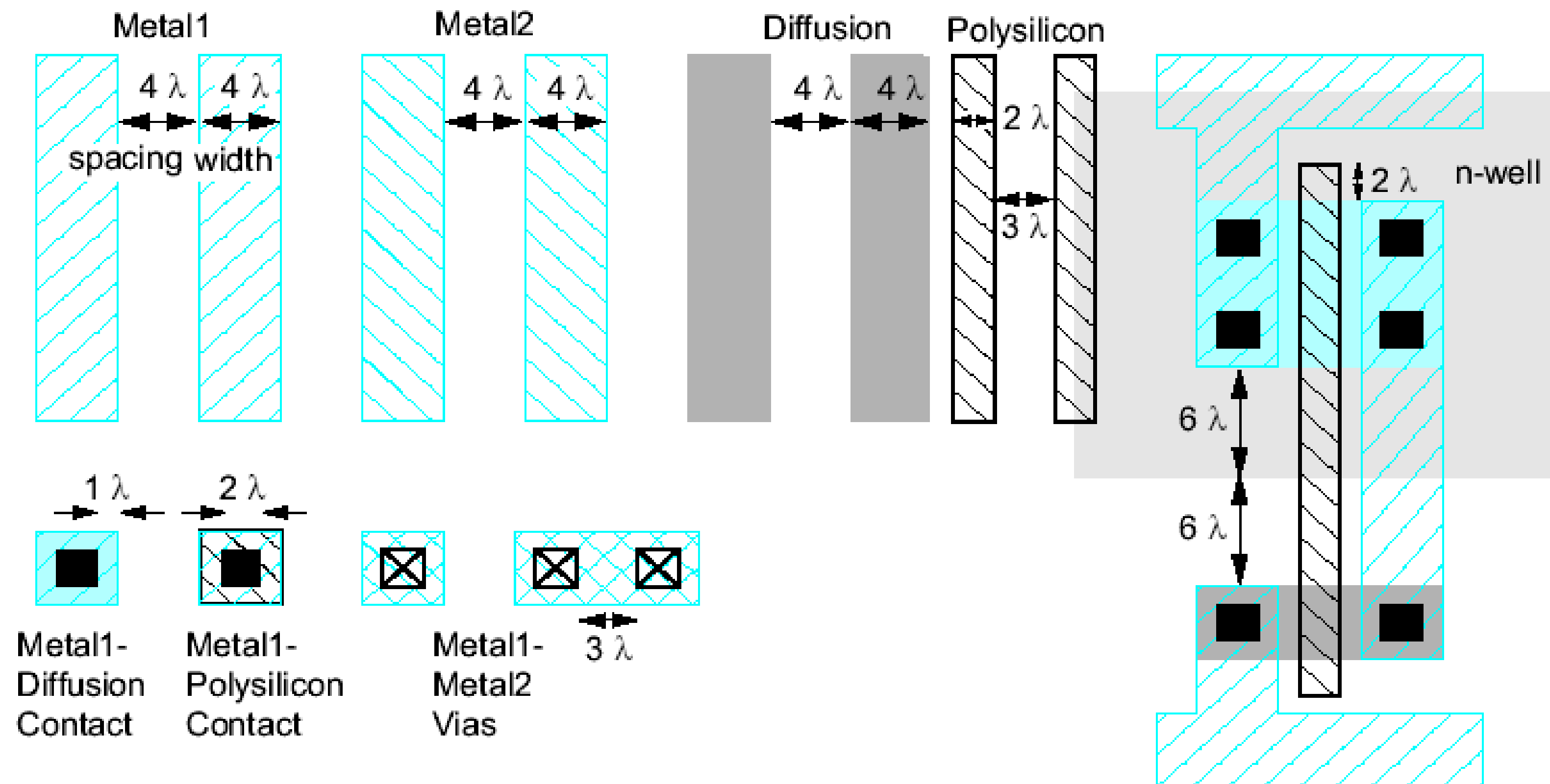


Layout

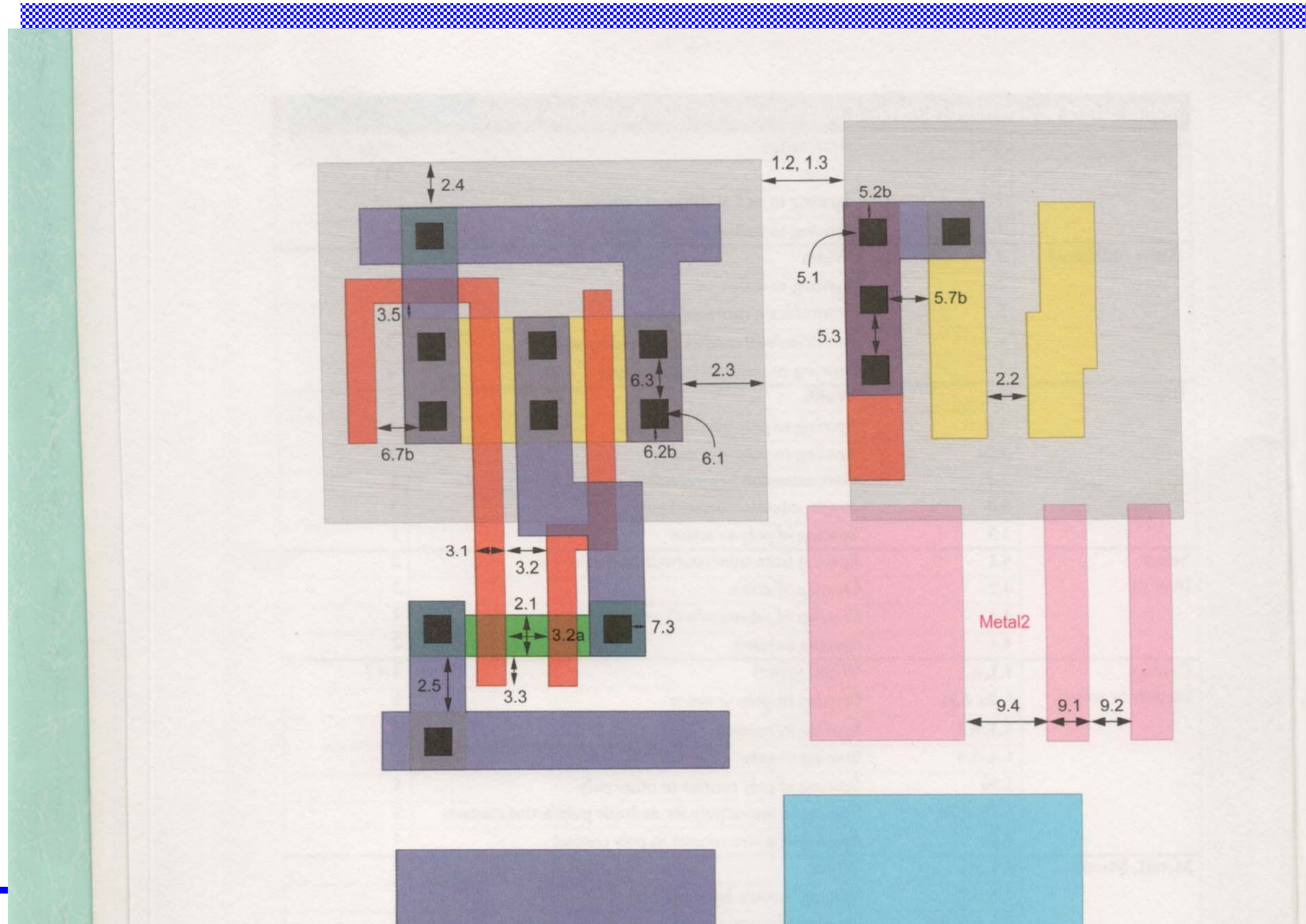
- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

Simplified Design Rules

- Conservative rules to get you started



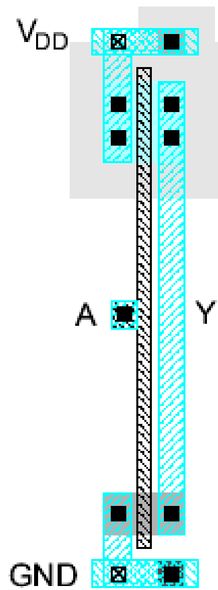
MOSIS Design Rules

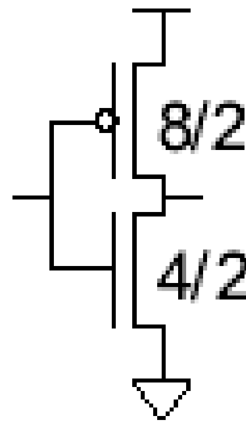


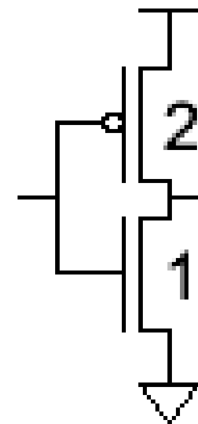
MOSIS SUBM design rules (3 metal, 1 poly with stacked vias & alternate contact rules)			
Layer	**Rule**	**Description**	**Rule (λ)**
N-well	1.1	Width	12
	1.2	Spacing to well at different potential	18
	1.3	Spacing to well at same potential	6
Active (diffusion)	2.1	Width	3
	2.2	Spacing to active	3
	2.3	Source/drain surround by well	6
	2.4	Substrate/well contact surround by well	3
	2.5	Spacing to active of opposite type	4
Poly	3.1	Width	2
	3.2	Spacing to poly over field oxide	3
	3.2a	Spacing to poly over active	3
	3.3	Gate extension beyond active	2
	3.4	Active extension beyond poly	3
	3.5	Spacing of poly to active	1
Select (n or p)	4.1	Spacing from substrate/well contact to gate	3
	4.2	Overlap of active	2
	4.3	Overlap of substrate/well contact	1
	4.4	Spacing to select	2
Contact (to poly or active)	5.1, 6.1	Width (exact)	2×2
	5.2b, 6.2b	Overlap by poly or active	1
	5.3, 6.3	Spacing to contact	3
	5.4, 6.4	Spacing to gate	2
	5.5b	Spacing of poly contact to other poly	5
	5.7b, 6.7b	Spacing to active/poly for multiple poly/active contacts	3
	6.8b	Spacing of active contact to poly contact	4
Metal1, Metal2	7.1, 9.1	Width	3
	7.2, 9.2	Spacing to same layer of metal	3
	7.3, 8.3, 9.3	Overlap of contact or via	1
	7.4, 9.4	Spacing to metal for lines wider than 10λ	6
Via1, Via2	8.1, 14.1	Width (exact)	2×2
	8.2, 14.2	Spacing to via on same layer	3
Metal3	15.1	Width	5
	15.2	Spacing to metal3	3
	15.3	Overlap of via2	2
	15.4	Spacing to metal for lines wider than $10\ \lambda$	6
Overglass Cut	10.1	Width of bond pad opening	60 μm

Inverter Layout

- Transistor dimensions specified as Width / Length
  - Minimum size is 4λ / 2λ, sometimes called 1 unit
  - In $f = 0.6$ μm process, this is 1.2 μm wide, 0.6 μm long







Summary

- MOS transistors are stacks of gate, oxide, silicon
- Act as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

- Now you know everything necessary to start designing schematics and layout for a simple chip!

About these Notes

- Lecture notes © 2010 David Money Harris
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