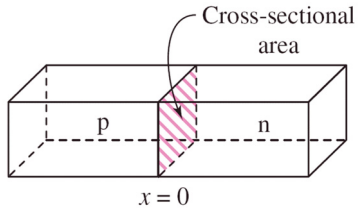
Overview of
Semiconductor Devices
(半導體元件概述)

- Specifically for NVM -

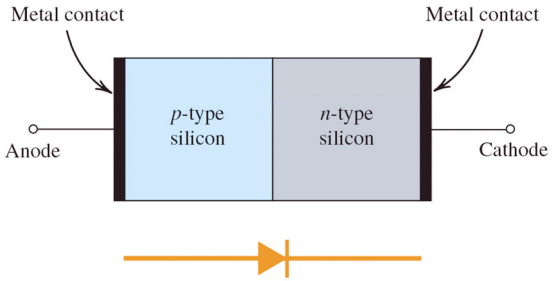
P-N Junction
Metal-Semiconductor Contact
MOS Capacitor
MOSFET
Nonvolatile Memory (NVM)

P-N Junction

p-n junction



p-n diode

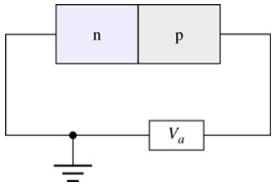


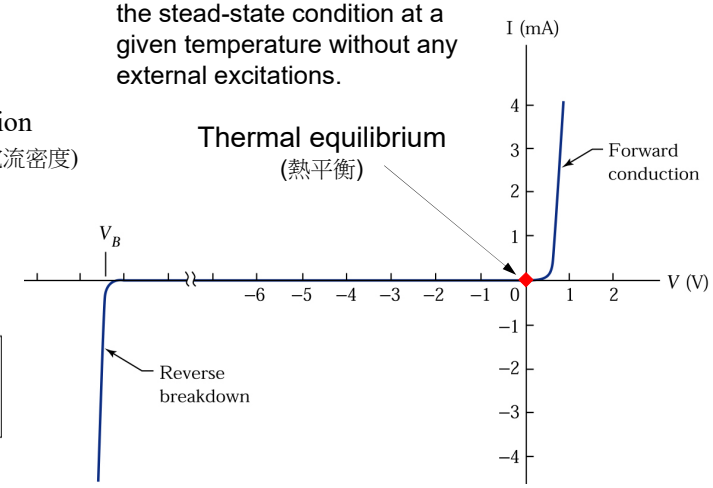
Ideal diode equation:

$\mathbf{J = J_s\,(e^{qV/kT} - 1)}$

where J_s is the saturation current density (飽和電流密度)

Thermal equilibrium:
the stead-state condition at a given temperature without any external excitations.





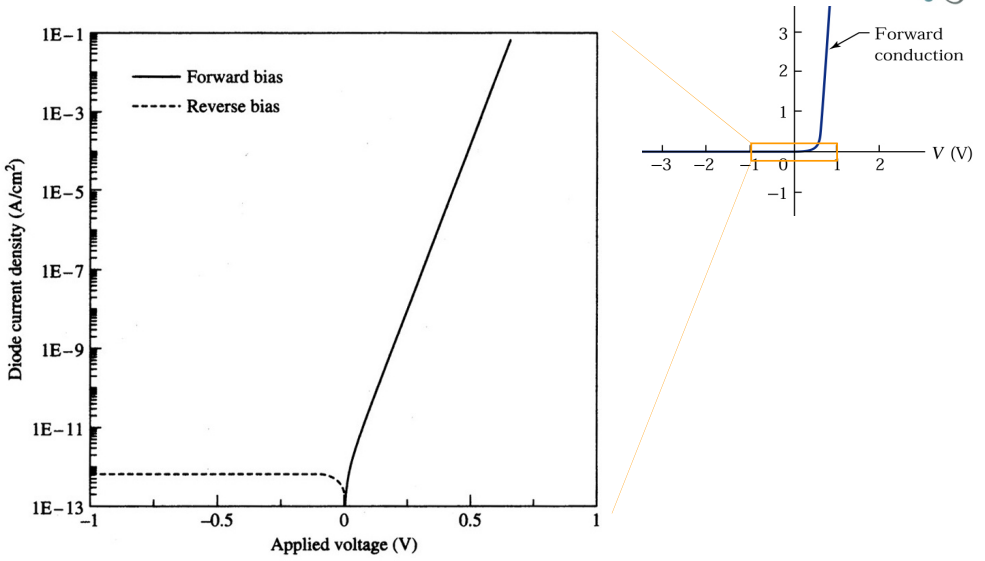
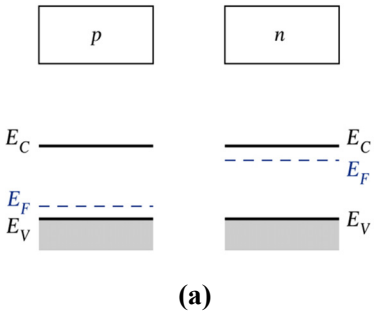


Fig. Current-voltage characteristics of a typical Si *p-n* junction.

Energy Band Diagram



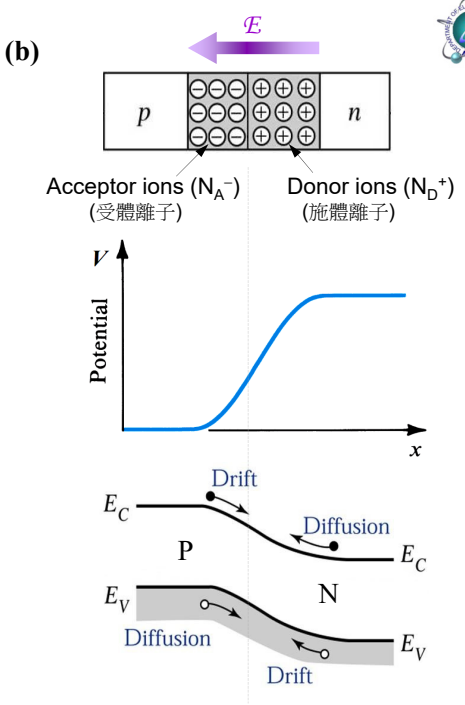
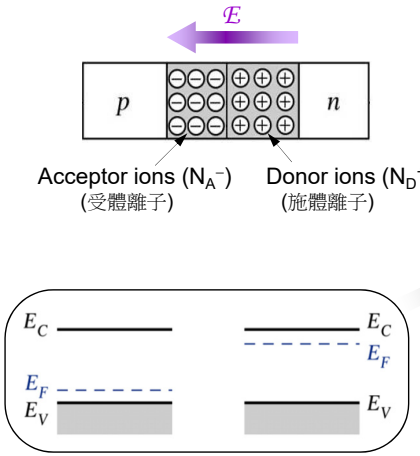
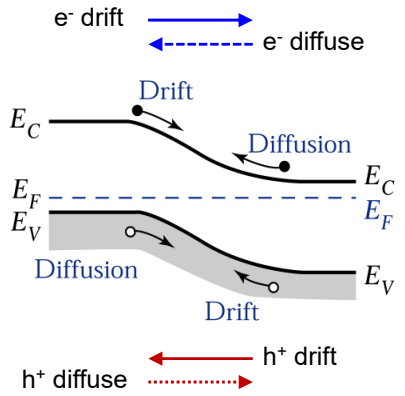


Fig.
(a) Uniformly doped *p*-type and *n*-type semiconductors before the junction is formed.
(b) The electric field in the depletion region and the energy band diagram of a *p*-*n* junction in thermal equilibrium.

- At thermal equilibrium, the individual electron and hole curent flowing across the junctions are identically zero, i.e., $J_n = 0$ and $J_p = 0$.
  $\Rightarrow$ **$\partial E_F/\partial x = 0$, i.e., the Fermi level $E_F(x)$ must be constant.**



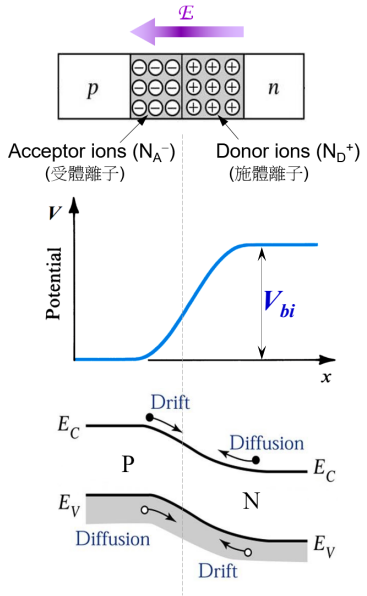


- **Built-in potential** (內植電位) or **built-in voltage** (內植電壓) = V_{bi}

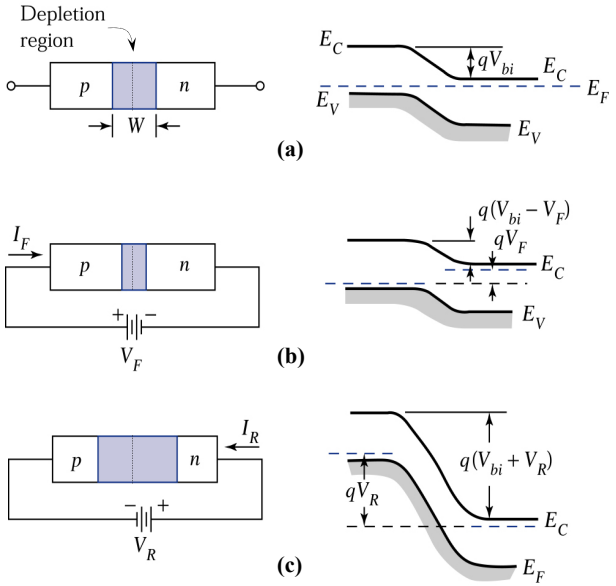
- $V_{bi} = \frac{kT}{q} ln\left(\frac{N_D N_A}{n_i^2}\right) = V_t ln\left(\frac{N_D N_A}{n_i^2}\right)$

  where q =1.6x10^{-19} C ;
  V_t (≡ kT/q) is called **thermal voltage** (熱電壓).

- At 300 K, kT = 0.0259 eV = 25.9 meV
  V_t = 0.0259 V = 25.9 mV



Depletion Region (空乏區)



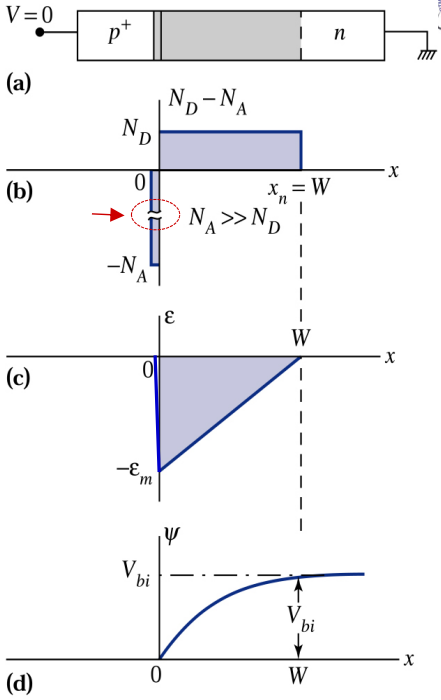
- Bias, V :
  $V_{bi} \rightarrow V_{bi} - V$
  Forward bias: V = V_F
  Reverse bias: V = $-V_R$
- The depletion width W becomes $\propto (V_{bi}-V)^{1/2}$.

Fig.
(*a*) In thermal equilbrium.
(*b*) Forward biased.
(*c*) Reverse biased.

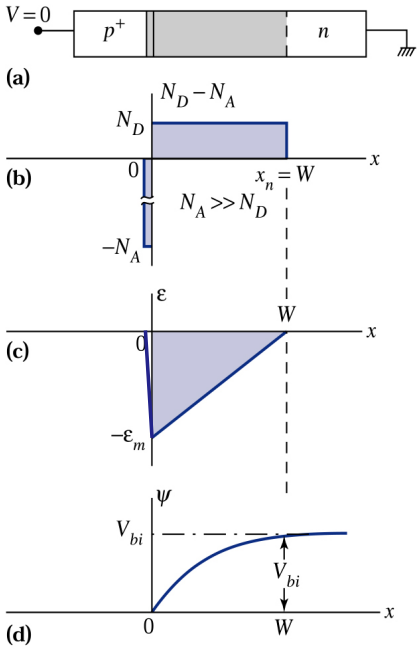
One-Sided Junction (單邊接面)

- One-sided junction:
  (單邊陡峭接面)
  $N_A >> N_D$ (or, $N_D >> N_A$)
  $\Rightarrow W \approx x_n$ (or, $W \approx x_p$)

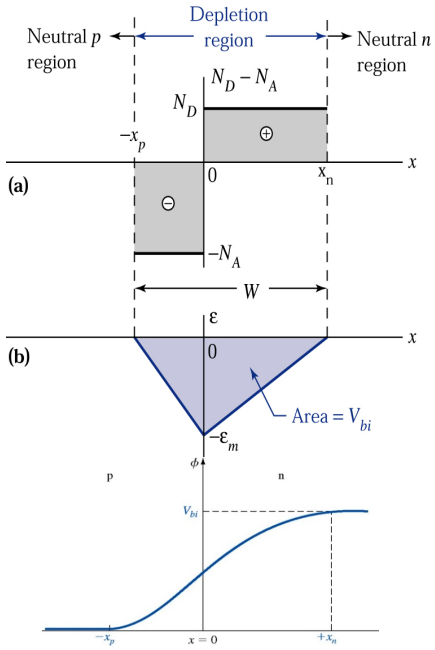
(a) One-sided abrupt junction (with $N_A >> N_D$) in thermal equilibrium.
(b) Space charge distribution.
(c) Electric-field distribution.
(d) Potential distribution with distance, where V_{bi} is the built-in potential.



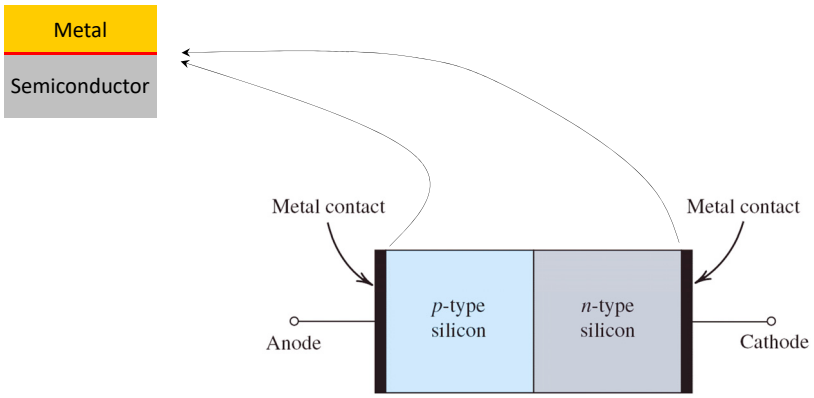
One-sided junction



General junction

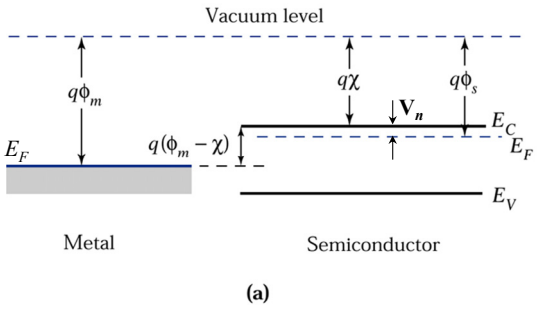


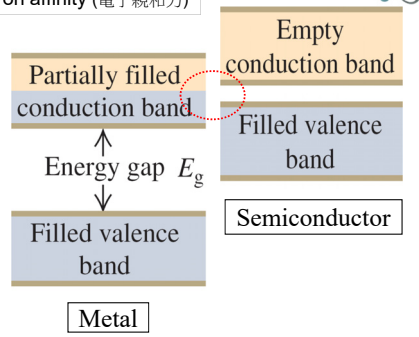
Metal-Semiconductor Contact (金屬-半導體接觸)



Basic Characteristics

$q\phi$: Work function (功函數)
$q\chi$: Electron affinity (電子親和力)



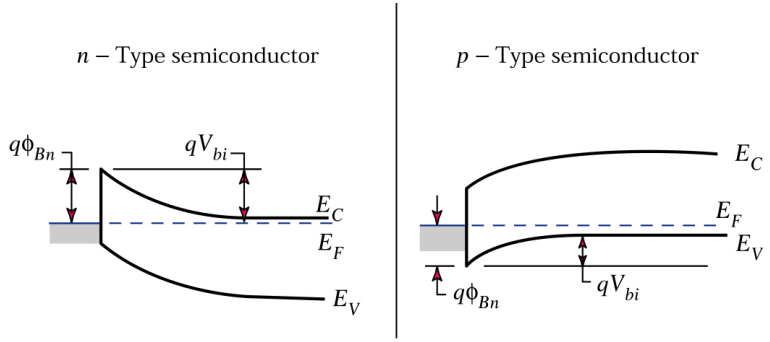


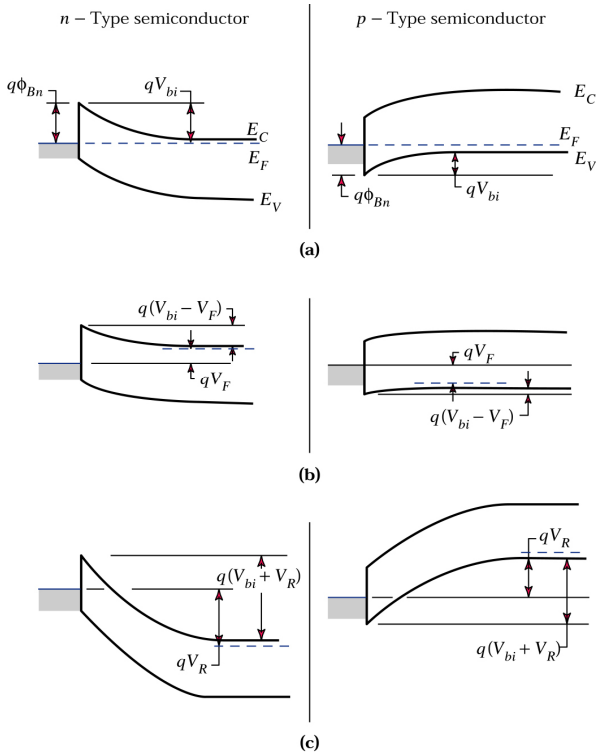
For n-type semiconductor:

- **Barrier height** (障壁高度) ← eV
  $q\phi_{Bn} = q\phi_m - q\chi$
- Built-in potential ← V
  $V_{bi} = \phi_{Bn} - V_n$

Fig. (*a*) Energy band diagram of an isolated metal adjacent to an isolated *n*-type semiconductor. (*b*) Energy band diagram in thermal equilibrium.

	n-type	*p-type*
Barrier height	$q\phi_{Bn} = q\phi_m - q\chi$	$q\phi_{Bp} = E_g - (q\phi_m - q\chi)$
	$q(\phi_{Bn} + \phi_{Bp}) = E_g$	
Built-in potential	$V_{bi} = \phi_{Bn} - V_n$	$V_{bi} = \phi_{Bp} - V_p$

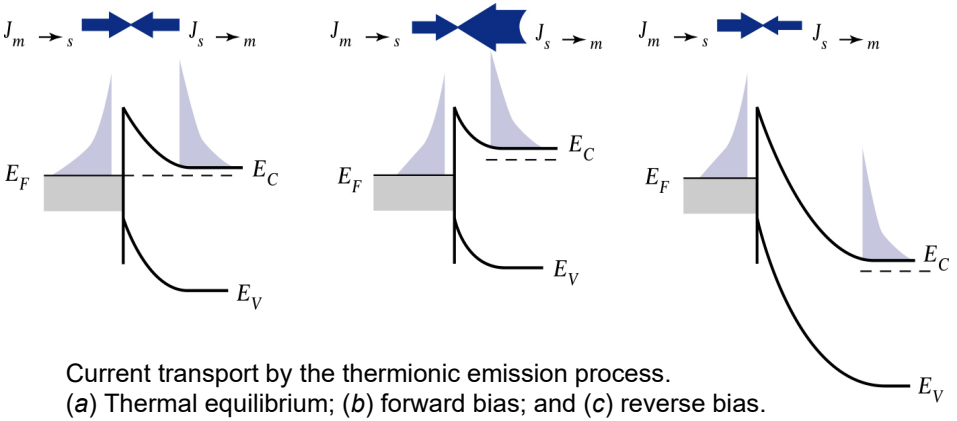




Energy band diagrams of metal *n*-type and *p*-type semiconductors under different biasing conditions: (*a*) thermal equilibrium; (*b*) forward bias; and (*c*) reverse bias.

Schottky Contact (蕭特基接觸)

- **Schottky barrier**: the barrier in the M-S contact with large ϕ_B and low doping.
- **Schottky diode**: M-S junction with a Schottky contact.
- Current transport → thermionic emission (熱離發射) of majority carriers.



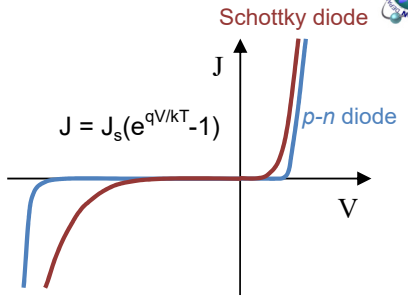
Current transport by the thermionic emission process.
(*a*) Thermal equilibrium; (*b*) forward bias; and (*c*) reverse bias.

- **Specific contact resistance** (特定接觸電阻), R_C

$$R_C \equiv \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \qquad \Omega \cdot cm^2$$

- **Contact resistance** (接觸電阻), R

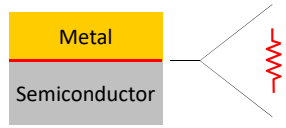
$$R = \left(\frac{\partial}{\partial V}\right)^{-1}_{V=0} = \left(A\frac{\partial J}{\partial V}\right)^{-1}_{V=0} = \frac{R_C}{A} \qquad \Omega$$



- For an M-S Schottky contact, in which the thermionic emission current dominates, we will have

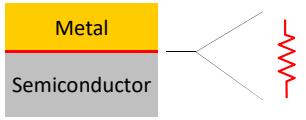
$$R_C = \frac{k}{qA^*T}\exp\left(\frac{q\phi_B}{kT}\right)$$

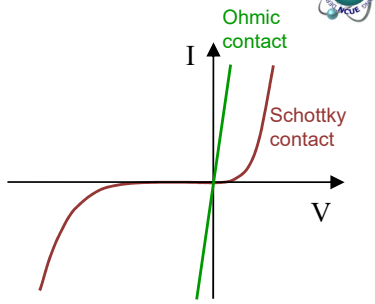
  - R_C normally is large due to the existence of ϕ_B.
  - Barrier height $\phi_B \downarrow \Rightarrow R_C$ & $R \downarrow$



Ohmic Contact (歐姆接觸)

- **Ohmic contact**: a M-S contact behaves like a *resistor of constant resistance*.





- To be a good ohmic contact, the M-S contact needs to have low R_c & R.

  ∴ A very low ϕ_B is necessary for a M-S contact in which thermionic emission dominates current transport.

  But, in practice, the barrier height ϕ_B is usually pinned at certain values and can not be controlled arbitrarily.

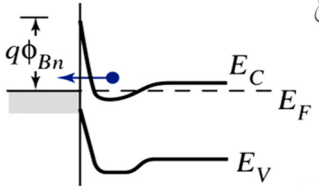
  ∴ Seeking the metal materials with very low ϕ_B to form ohmic contact is an impractical approach.

- The effective approach to form ohmic contact is to use "tunneling (穿隧)" instead of "thermionic emission" as the current transport mechanism.

- High doping concentration.

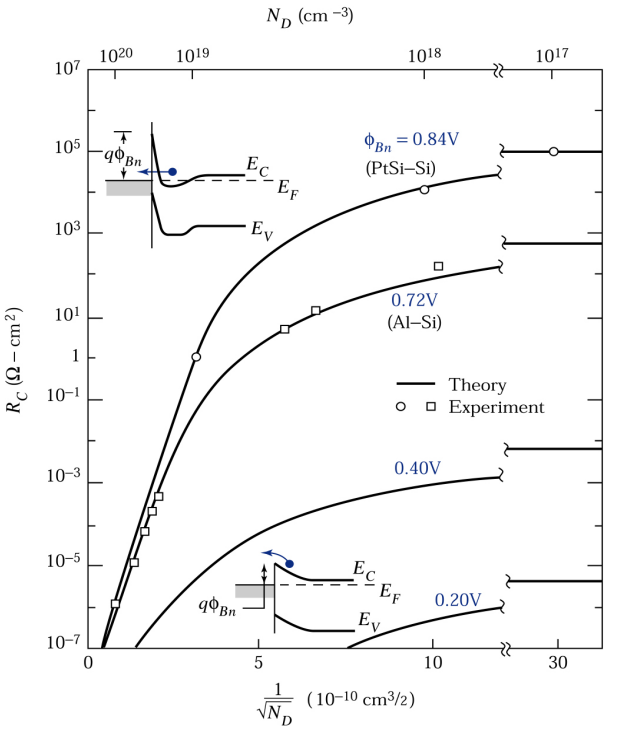
  ⇒ Very narrow barrier width.

  ⇒ **Tunneling** (穿隧) current dominates.



- The specific contact resistance is

$$R_C \sim \exp\left(\frac{C_2\phi_{Bn}}{\sqrt{N_D}}\right) = \exp\left(\frac{4\sqrt{m_n\varepsilon_s}}{\sqrt{N_D}}\frac{\phi_{Bn}}{\hbar}\right). \quad \propto \exp(\phi_{Bn}/N_D^{1/2})$$



Calculated and measured values of specific contact resistance. Upper inset shows the tunneling process. Lower inset shows thermionic emission over the low barrier.

MOS Capacitor

- MOS = Metal-Oxide-Semiconductor (金氧半)
- The MOS capacitor is very important!
  -- study of semiconductor surfaces.
  -- heart of MOSFET (metal-oxide-semiconductor field-effect transistor).
  -- a storage capacitor in IC.
  -- the basic building block for CCD.

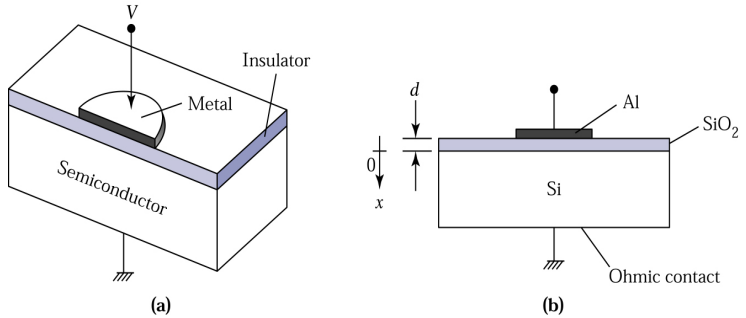


Fig. (*a*) Perspective view of a metal-oxide-semiconductor (MOS) capacitor. (*b*) Cross-section of a Si MOS capacitor.

Ideal MOS Capacitor

An ideal MOS is defined as follows:

a) ***Flat-band condition*** (平帶狀態) at V=0, i.e., $q\phi_{ms} \equiv q\phi_m - q\phi_s = 0$

b) The only charges which exist under bias are:
- charges in the semiconductor, and
- charges equal but with opposite sign on the metal surface adjacent to the oxide.

c) Infinite oxide resistivity: no carrier transport through the oxide under DC bias.

$q\phi$: Work function (功函數)

$q\chi$: Electron affinity (電子親和力)

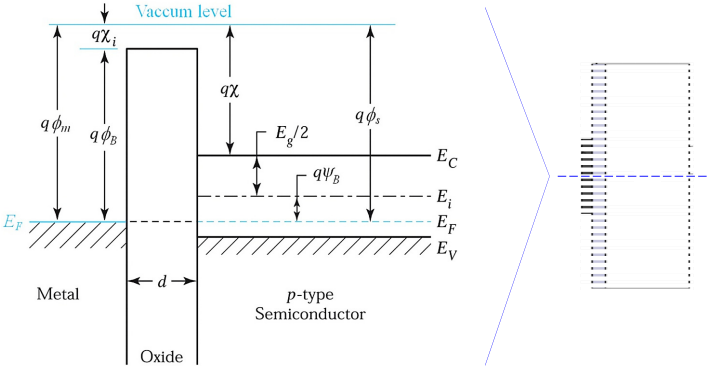


Fig. Energy band diagram of an ideal MOS capacitor at $V = 0$.

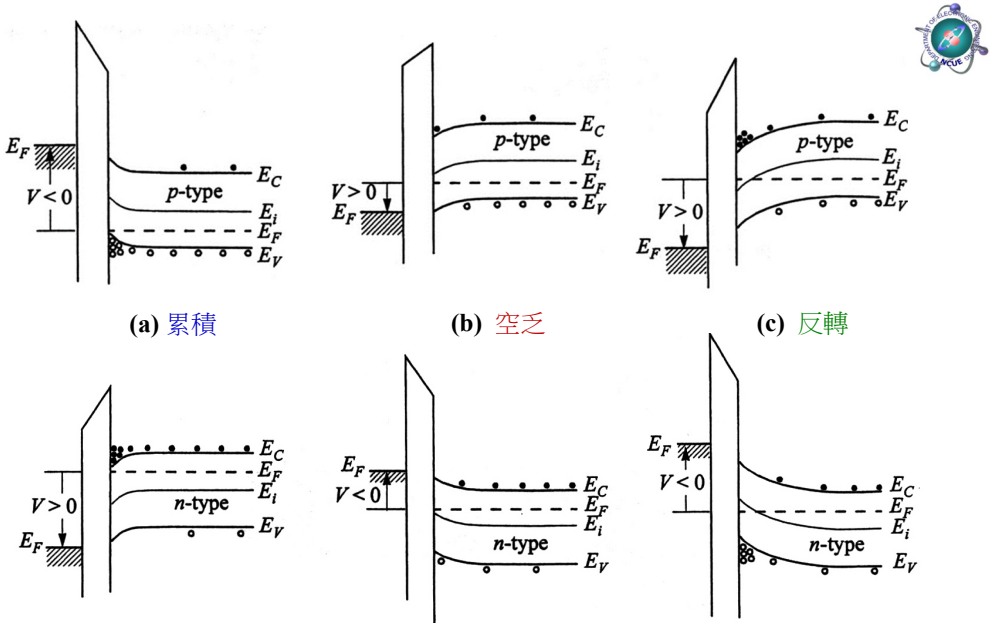


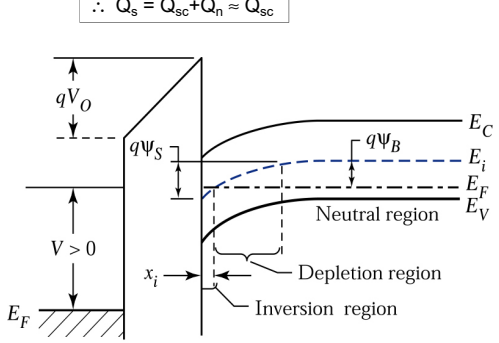
Fig. Energy-band diagrams for ideal MIS capacitors under different bias, for the conditions of: (a) accumulation, (b) depletion, and (c) inversion. Top/bottom figures are for *p*-type/*n*-type semiconductor substrates.

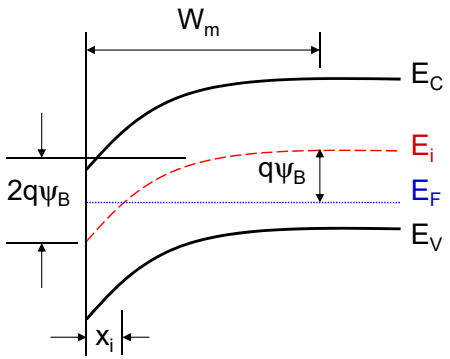
- ***Threshold voltage*** (臨界電壓) or ***Turn-on voltage*** (起始電壓), V_T ≡ Applied gate voltage V_G at the onset of strong inversion
- We have

$$V_T = (V_o + \psi_s)_{(inversion)} = (\mathcal{E}_o d + \psi_s)_{(inversion)} = \frac{|Q_s|_{(inversion)}}{C_o} + 2\psi_B$$

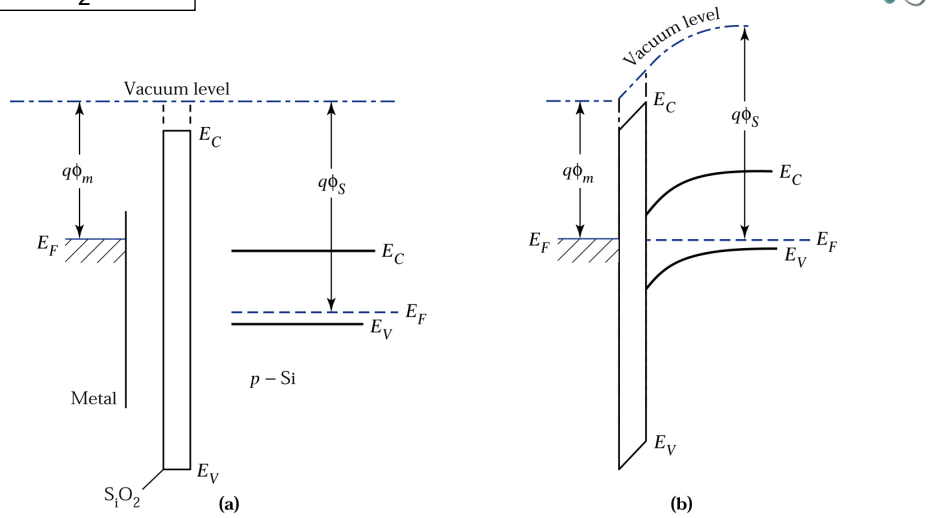
$$\approx \frac{|Q_{sc}|_{(inversion)}}{C_o} + 2\psi_B = \frac{qN_A W_m}{C_o} + 2\psi_B = \frac{\sqrt{2\varepsilon_s qN_A(2\psi_B)}}{C_o} + 2\psi_B$$

$Q_{sc} = -qN_A W_m$
$Q_n = -qN_A x_i$
$|Q_{sc}| >> |Q_n|$
$\therefore\ Q_s = Q_{sc}+Q_n \approx Q_{sc}$



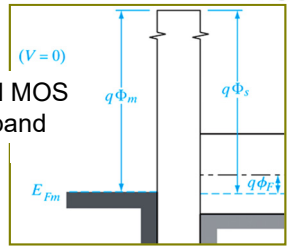


Si-SiO_2 MOS

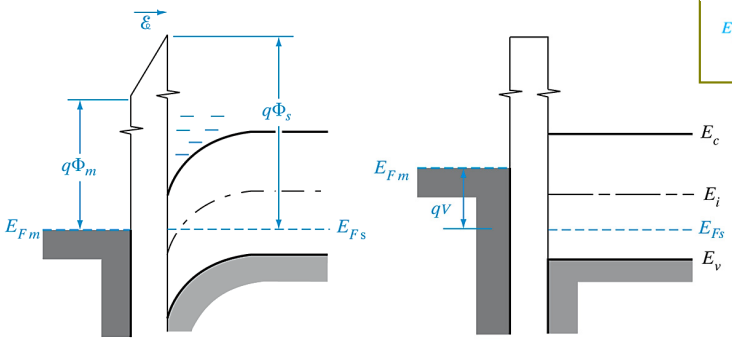


(*a*) Energy band diagram of an isolated metal and an isolated semiconductor with an oxide layer between them. (*b*) Energy band diagram of an MOS capacitor in thermal equilibrium.

- **Flat-band voltage** (平帶電壓) V_{FB} :
  the voltage to get the energy band diagram (a) to the flat-band condition (b).
  ∴ $V_{FB} = \phi_{ms}$ ($= \phi_m - \phi_s$)
- Practical V_T = Ideal V_T + V_{FB}



Ideal MOS flat band

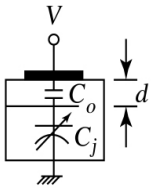


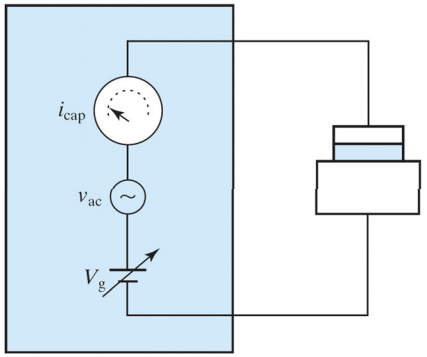
(a) Equilibrium $V = 0$ (b) Flat band $V = V_{FB} = \Phi_{ms}$

Effect of a negative work function difference ($\Phi_{ms} < 0$): (a) band bending and formation of negative charge at the semiconductor surface; (b) achievement of the flat band condition by application of a negative voltage.

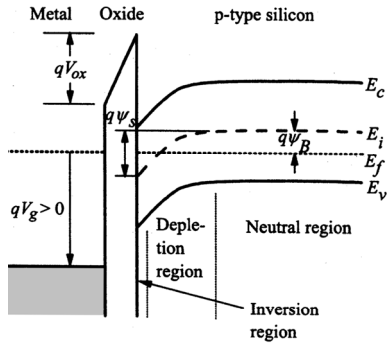
Capacitance in an MOS Structure

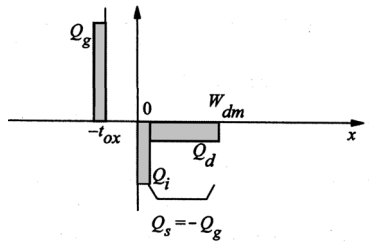
- $C_o = \varepsilon_{ox} / t_{ox}$ ← fixed
  $C_j = \varepsilon_s / W_d$ ← V dependent
- $\frac{1}{C} = \frac{1}{C_o} + \frac{1}{C_j}$





C–V meter MOS capacitor

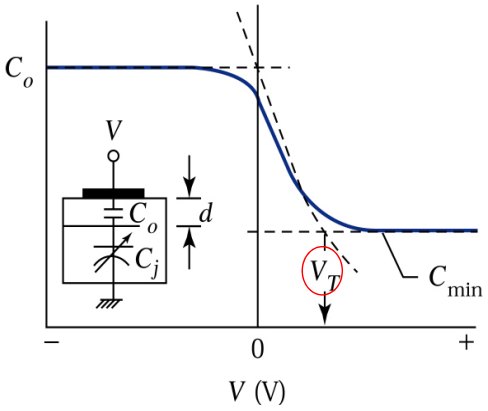




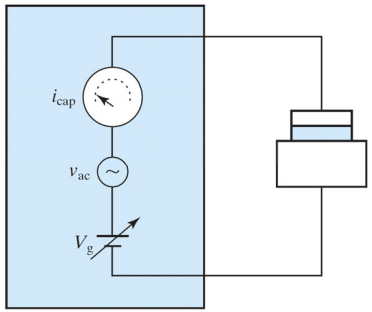
- Total capacitance C.
  $1/C = 1/C_o + 1/C_j$
  $\Rightarrow C = C_o C_j / (C_o + C_j)$
- Accumulation ($V < 0$):
  No depletion region ⇒ No C_j
  ∴ $C = C_o = \varepsilon_{ox} / d$
- Depletion ($V > 0$):

$$\Rightarrow \frac{C}{C_0} = \frac{1}{\sqrt{1 + \frac{2\varepsilon_{ox}^2 (V - V_{fb})}{qN_A \varepsilon_s d^2}}}$$

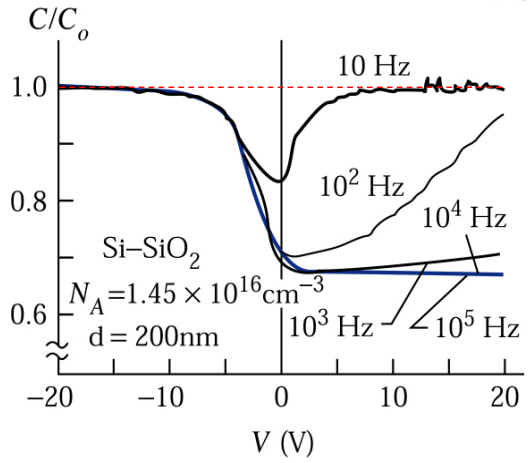
- Strong inversion ($V >> 0$):
  $C_j = \varepsilon_s / W_m$, $C_o = \varepsilon_{ox} / d$
  ∴ $C \equiv C_{min} = \varepsilon_{ox} / [d + (\varepsilon_{ox}/\varepsilon_s) W_m]$
  $= \varepsilon_s / [d(\varepsilon_s/\varepsilon_{ox}) + W_m]$



(High-frequency) MOS *C-V* curve showing its approximated segments (dashed lines). Inset shows the series connection of the capacitors.

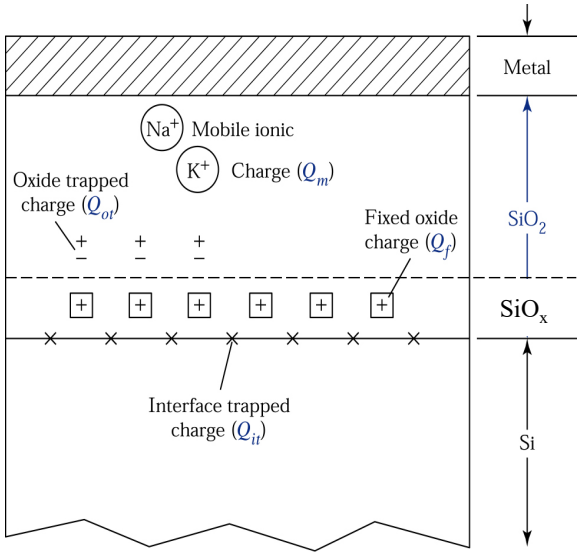


C–V meter MOS capacitor



Effect of measurement frequency on the *C-V* curve.

Interface Traps (介面陷阱) and Oxide Charges (氧化層電荷)



Charges and their location in thermally oxidized silicon.

- Interface:
  Interface-trapped charge, Q_{it}
- Inside bulk:
  Fixed oxide charge, Q_f
  Oxide-trapped charge, Q_{ot}
  Mobile ionic charge, Q_m

⇑

Effective net charges per unit area (C/cm^2)

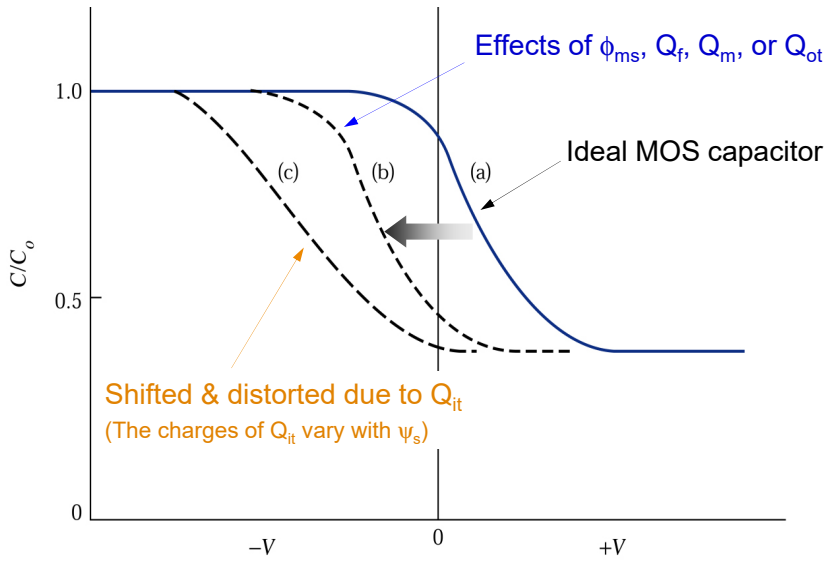


Fig. (a) The C-V characteristics of an ideal MOS capacitor. (b) Parallel shift along the voltage axis due to positive fixed oxide charges. (c) Nonparallel shift along the voltage axis due to interace traps..

- For an arbitary volume charge density in oxide, ρ(x) ← unit: C/cm^3
- $\Delta Q_o(x) = \rho(x)\Delta x \Rightarrow \Delta V_{FB} = -(\Delta Q_o/C_{ox})(x/d) = -[(\rho(x)\Delta x)/C_{ox}](x/d)$

$$\therefore V_{FB} = \int_0^d dV_{FB} = \int_0^d -\frac{\rho(x)dx}{C_{ox}}\frac{x}{d} = -\frac{1}{C_{ox}}\left[\frac{1}{d}\int_0^d x\rho(x)dx\right] = -\frac{1}{\varepsilon_{ox}}\int_0^d x\rho(x)dx$$

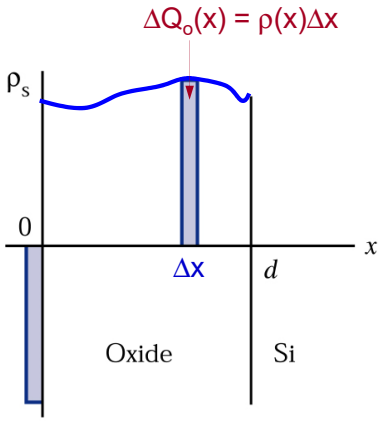
- $$Q_{ot} \equiv \frac{1}{d}\int_0^d x\rho_{ot}(x)dx$$
  $$Q_m \equiv \frac{1}{d}\int_0^d x\rho_m(x)dx$$
- If $q\phi_{ms} \neq 0$ and Q_{it} is ignored,

$$V_{FB} = \phi_{ms} - \frac{(Q_f + Q_m + Q_{ot})}{C_{ox}}$$

- Practical V_T = Ideal V_T + V_{FB}

$$= \psi_s + \frac{|Q_s|}{C_o} + V_{FB}$$

$$= 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_o} + V_{FB}$$



Conduction Processes in Oxide

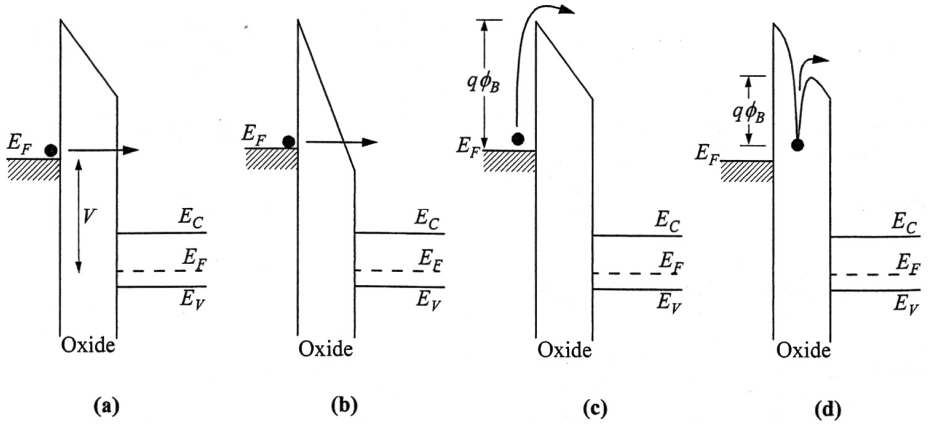
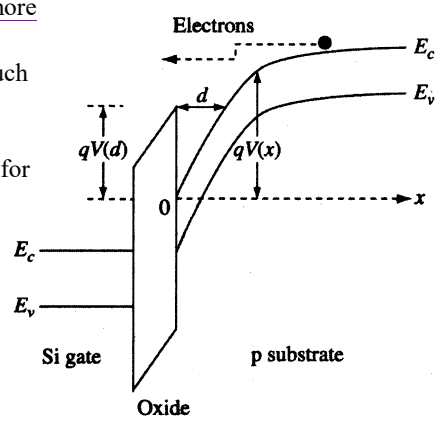


Fig. Energy band diagrams showing conduction mechanisms of (a) direct tunneling, (b) Fowler-Nordheim tunneling, (c) thermionic emission, and (d) Frenkel-Poole emission.

Injection of Hot Carriers (熱載子) from Si to SiO_2

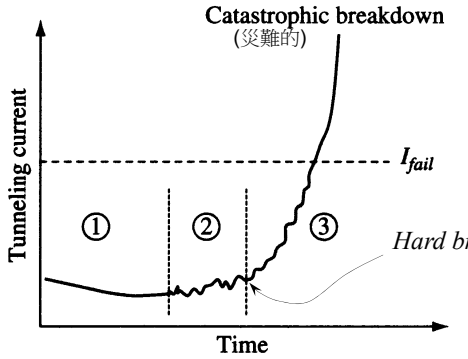
- "Hot" carrier: the carrier with high kinetic energy (動能).
- If a region of sufficiently high electric field is located near the Si-SiO_2 interface, some electrons or holes in the region can gain enough kinetic energy from the electric field to surmount (越過) the interface barrier and enter the SiO_2 layer.
- Injection from Si into SiO_2 is , in general, much more likely for hot electrons than for hot holes because
  1) electrons gain energy from the electric field much more readily than holes due to their smaller effective mass, and
  2) The Si-SiO_2 interface energy barrier is smaller for electrons (~3.1 eV) than for holes (~4.6 eV).

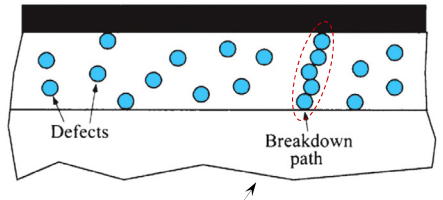


Dielectric Breakdown (介電崩潰)

3 stages of the tunneling current in a modern thin-oxide MOS device:

① *Defect generation* (缺陷產生) or *Stress-induced leakage current* (應力引致漏電流)
② *Soft breakdown* (軟崩潰).
③ *Successive breakdown* (接續崩潰) or *Progressive breakdown* (循序崩潰)





- Two measures to quantify reliability:
  1) ***Time to breakdown*** t_{BD} : total stress time until breakdown occurs.
  2) ***Charge to breakdown*** q_{BD}: total charge (integrating the current) passed through the device within t_{BD}.
- t_{BD} and q_{BD} are both functions of applied bias.

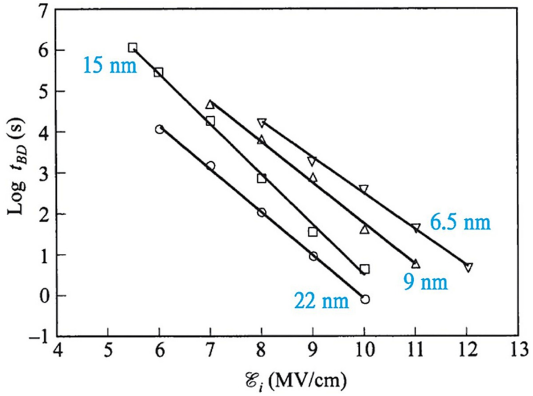
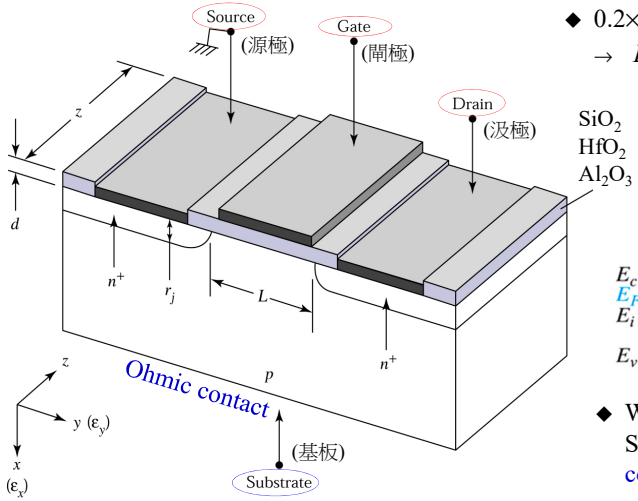
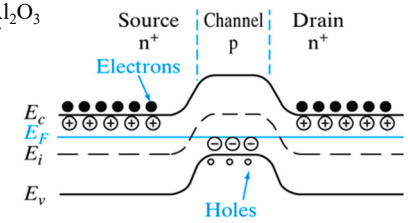


Fig. Time to breakdown t_{BD} vs. oxide field for different oxide thicknesses.

MOSFET



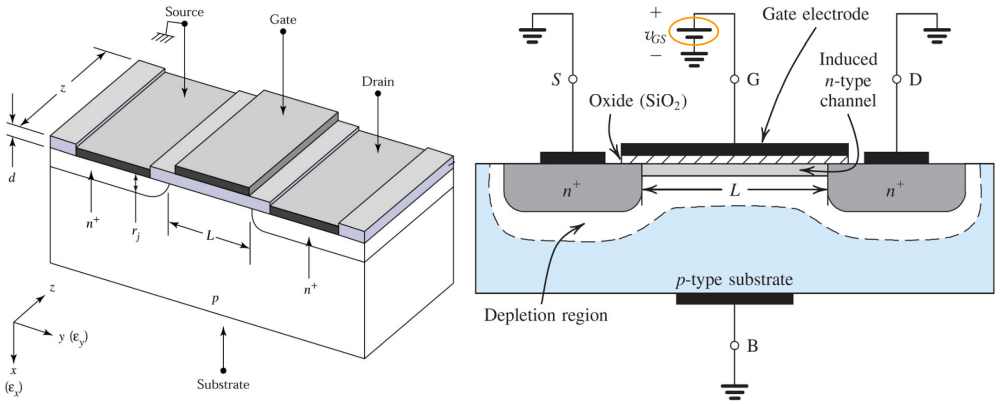
- L : channel length (通道長度)
  z : channel width (通道寬度)
- 0.2×100 μm device
  → L = 0.2 μm, z = 100 μm

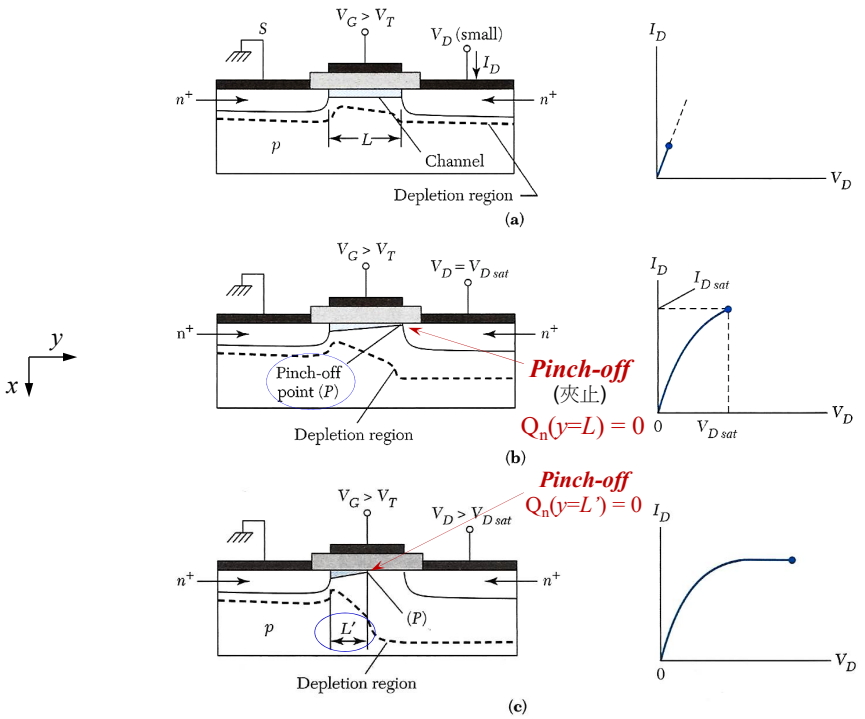


- When without V_G : the path between S and D is like two p-n junctions connected back to back.
  ⇒ Only reverse leakage current.

Fig. Perspective view of a metal-oxide-semiconductor field-effect transistor (MOSFET) (金氧半場效電晶體).

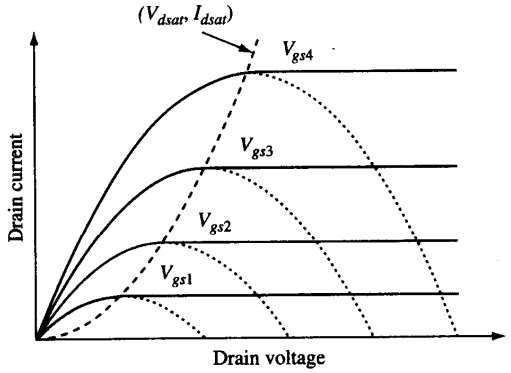
- V_G large enough ⇒ Surface inversion layer (i.e., conduction channel) is formed.
- Depletion regions are formed:
  - S & D n^+-p junctions.
  - Depletion layer alongside the inversion channel layer.
- Substrate bias also affects the channel conductance.





I-V Characteristics

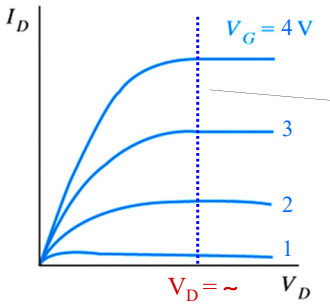
$$I_D \approx \frac{W}{L}\mu_{eff}C_{ox}\left\{\left(V_G - V_{FB} - 2\psi_B - \frac{V_D}{2}\right)V_D - \frac{2}{3}\frac{\sqrt{2\varepsilon_s qN_A}}{C_{ox}}\left[(V_D + 2\psi_B)^{3/2} - (2\psi_B)^{3/2}\right]\right\}$$

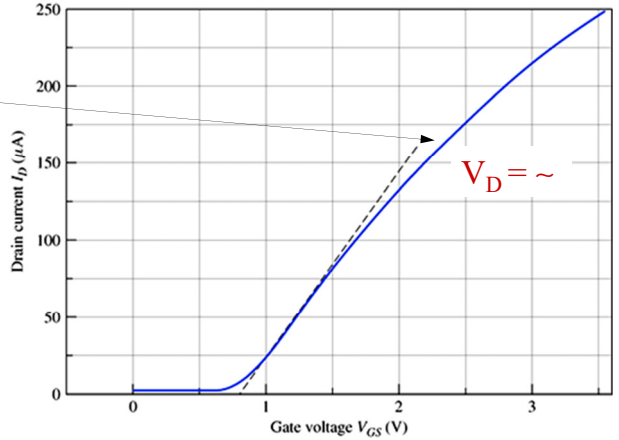


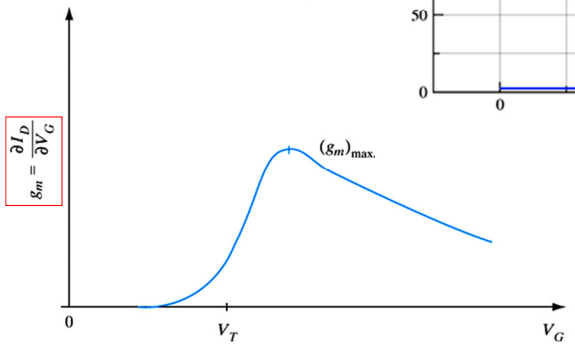
- **Conductance** (電導)
  $g_D \equiv (\partial I_D/\partial V_D)\,|_{V_G=\text{constant}}$
  Transconductance (轉導)
  $g_m \equiv (\partial I_D/\partial V_G)\,|_{V_D=\text{constant}}$

Long-channel MOSFET I_{ds} –V_{ds} characteristics (solid curves) for several different values of V_{gs}. The dashed curve shows the trajectory of drain voltage beyond which the current saturates. The dotted curves help to illustrate the parabolic behavior of the characteristics before saturation.

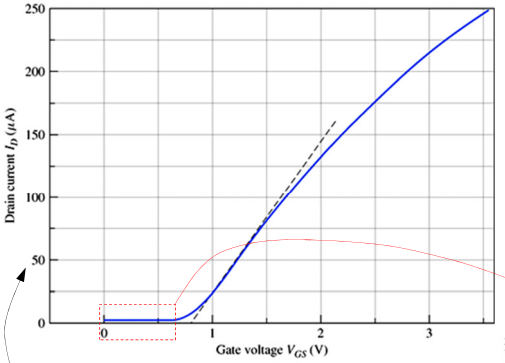
Transfer characteristics (轉換特性曲線), $I_D - V_G$





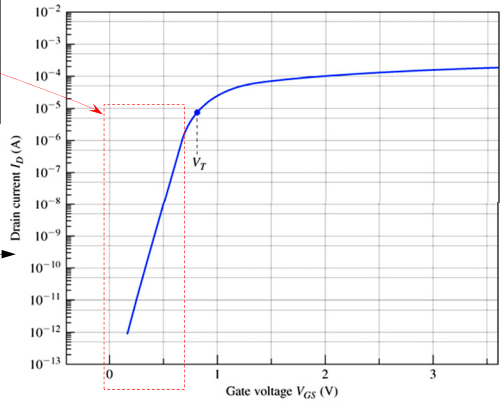


Conductance (電導)
$g_D \equiv (\partial I_D/\partial V_D)\,|_{V_G=\text{constant}}$
Transconductance (轉導)
$g_m \equiv (\partial I_D/\partial V_G)\,|_{V_D=\text{constant}}$

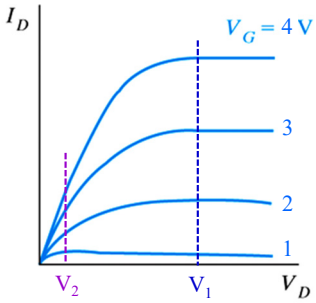


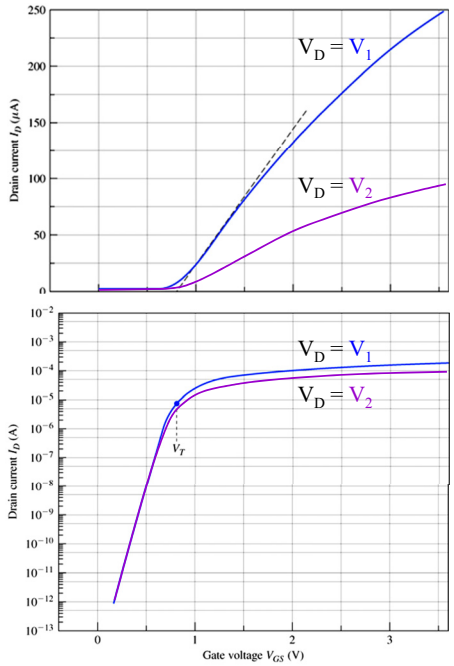
Linear scale

Semilog plot (半對數繪圖)



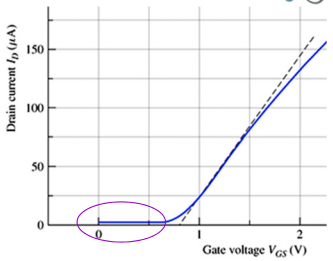
Logarithmic (對數的) scale,
or simply "Log scale"
<Note> log_{10} , not log_e

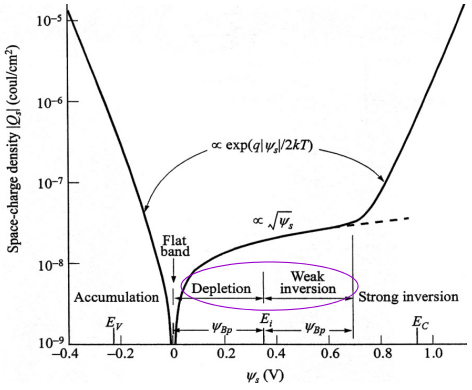


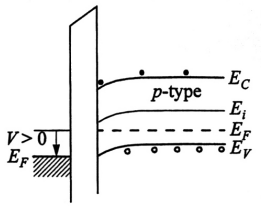


Subthreshold region (次臨界區域)

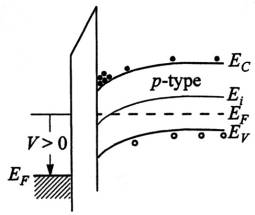
- ***Subthreshold region***:
  $V_G < V_T$ & semiconductor surface is in weak inversion or depletion (i.e., when $0 \le \psi_s < 2\psi_B$).





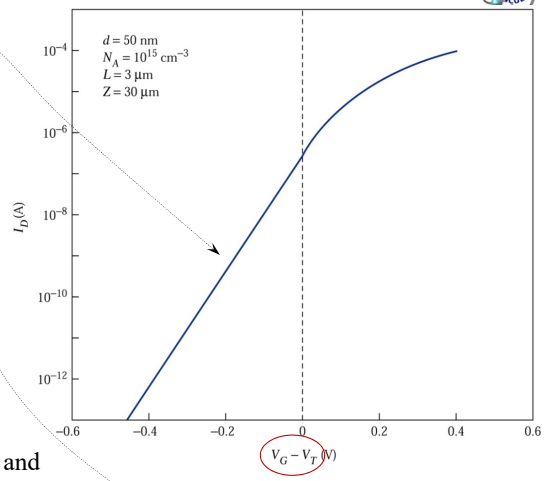


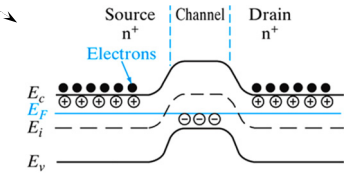
Depletion



Weak inversion

- ***Subthreshold current***, I_{Sub}
- Drain current is dominated by carrier diffusion (instead of carrier drift).
  $I_D \propto e^{q(V_G - V_T)/kT} \cdot [1 - e^{-qV_D/kT}]$
- ***Subthreshold swing (slope)***:
  (次臨界擺幅(斜率))
  $S \equiv \left[\frac{\partial(\log I_D)}{\partial V_G}\right]^{-1}$ *(mV/decade)*
- $S = ln(10)\left(\frac{kT}{q}\right)\left(\frac{C_o + C_D + C_{it}}{C_o}\right)$
  $\approx 2.303\left(\frac{kT}{q}\right)\left(1 + \frac{C_D + C_{it}}{C_o}\right)$
  where C_D is the depletion capacitance, and
  C_{it} ($= q^2 \cdot D_{it}$) is the capacitance due to D_{it}.
- At 300 K: $S \approx 60\left(1 + \frac{C_D + C_{it}}{C_o}\right)$ *mV/decade*.
  Typically S = 70~100 *mV/decade*





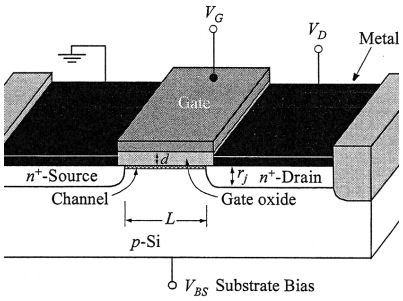
Threshold Voltage (臨界電壓)

- V_T is one of the most important parameters of MOSFETs.
- Ideal $V_T = [2\varepsilon_s q N_A (2\psi_B)]^{1/2}/C_{ox} + 2\psi_B$
- Practical V_T = Ideal $V_T + V_{FB}$

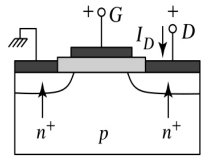
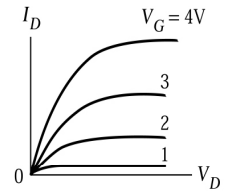
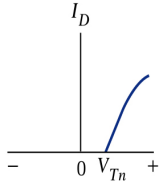
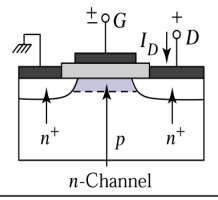
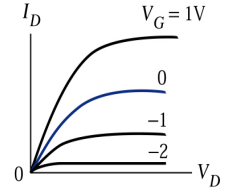
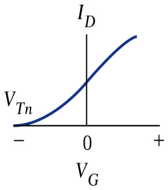
  $\approx 2\psi_B + [2\varepsilon_s q N_A (2\psi_B - V_{BS})]^{1/2}/C_{ox} + V_{FB}$

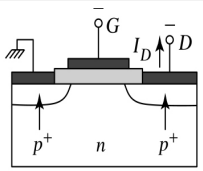
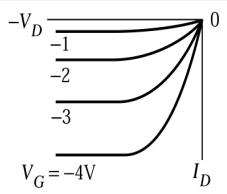
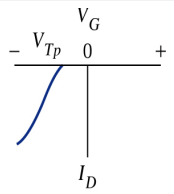
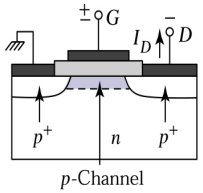
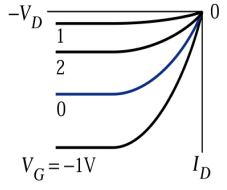
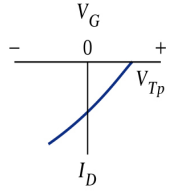
  (V_{BS} is the substrate bias voltage.)

where $V_{FB} = \phi_{ms} - \dfrac{(Q_f + Q_m + Q_{ot})}{C_o}$



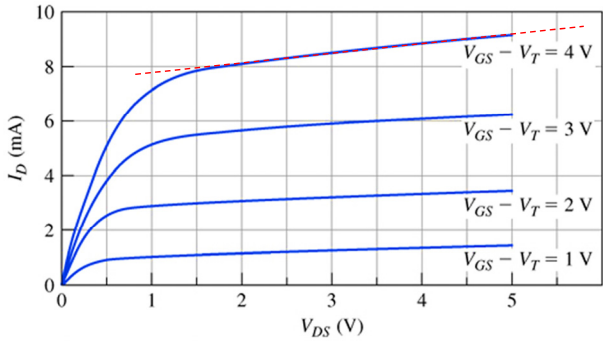
Types of MOSFETs

Type	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)			
n-Channel Depletion (Normally On)			

Type	Cross Section	Output Characteristics	Transfer Characteristics
p-Channel Enhancement (Normally Off)			
p-Channel Depletion (Normally On)			

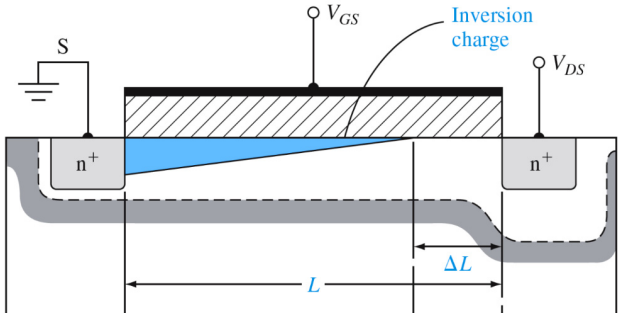
Channel Length Modulation (通道長度調變)

- The drain current of a short-channel MOSFET can still increase slightly beyond the pinch-off or the velocity saturation point, resulting in a non-zero output conductance.
- This arises due to two factors:
  1) short-channel effect, which gives V_T to decrease after V_D increases beyond saturation.
  2) channel length modulation.



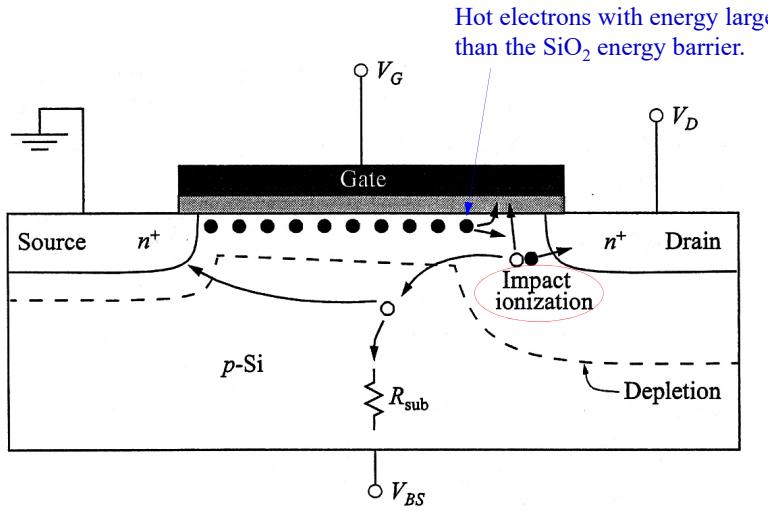
- Effective channel length (有效通道長度) = L − ΔL.
- $I_D' = \left(\frac{L}{L-\Delta L}\right) I_D$

  I_D' is the actual current and I_D is the ideal current.

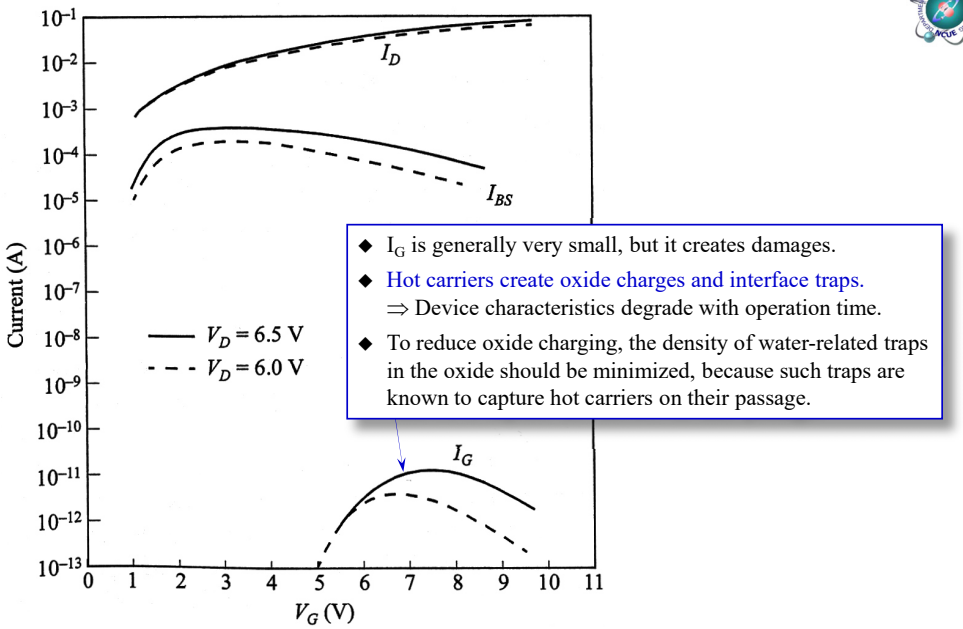


Energy band diagrams for qualitative explanation of channel-length modulation.

Device Degradation & Breakdown at High Fields

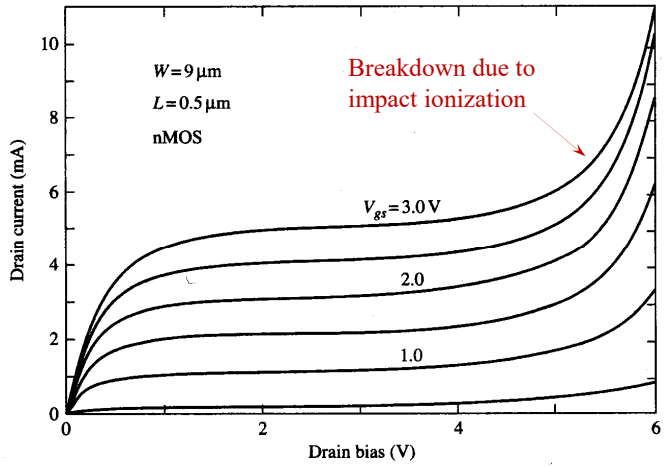


Current components of a MOSFET under high fields.



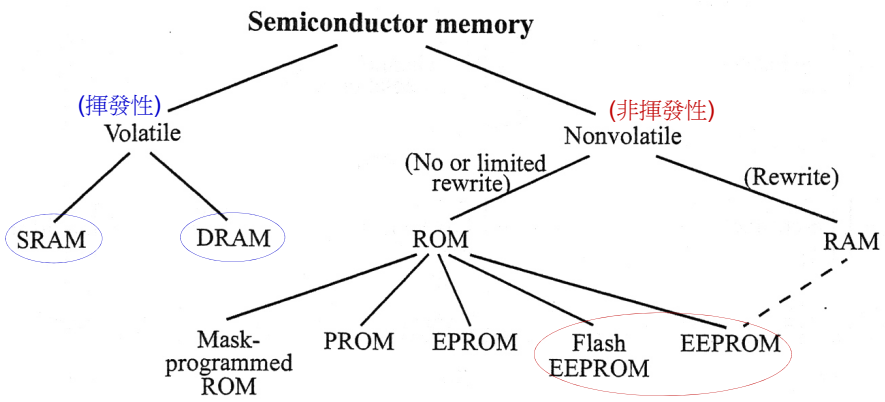
- I_G is generally very small, but it creates damages.
- Hot carriers create oxide charges and interface traps.
  ⇒ Device characteristics degrade with operation time.
- To reduce oxide charging, the density of water-related traps in the oxide should be minimized, because such traps are known to capture hot carriers on their passage.

Drain current, substrate current, and gate current vs. gate voltage of a MOSFET. L/W = 0.8/30 μm.



Example $I_{ds} - V_{ds}$ curves of a short-channel nMOSFET showing breakdown at high drain voltages.

Nonvolatile Memory (NVM) (非揮發性記憶體)

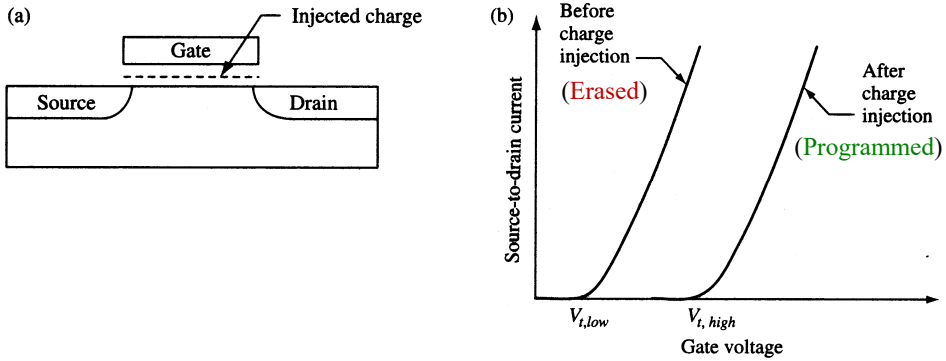


NVM

- Any bistable device that retains its state when the power supply is disconnected can make a nonvolatile memory cell.
- ***Programmable read-only memory*** (PROM) (可程式唯讀記憶體): memory cells can not be reprogrammed.
- ***Erasable programmable read-only memory*** (EPROM) (可抹除可程式唯讀記憶體): memory cells can be erased and reprogrammed.
  - The memory erasure is done by non-electrical means (e.g., exposure to UV light).
- ***Electrically erasable programmable read-only memory*** (EEPROM) (電性式可抹除可程式唯讀記憶體): memory cells can be erased electrically and reprogrammed.
  - Now interchangeably so-called "***Flash memory***" (快閃記憶體), named due to its fast erasing action.
- The technical considerations of NVM are:
  1) Memory speed
  2) Memory retention time (記憶存留時間)
  3) Memory endurance time (記憶耐受時間)
  4) Power dissipation (功率消耗)
  5) Power supply voltage
  6) Memory cell size
  7) Scaling properties of the memory technology

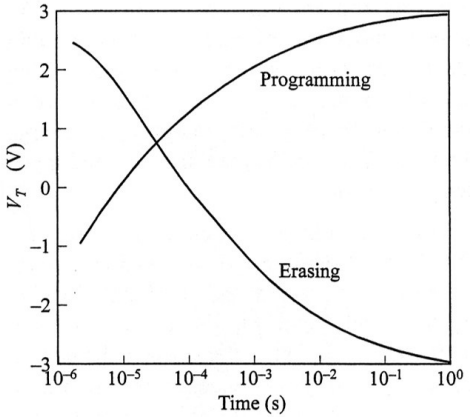
Basic Principles of NVM

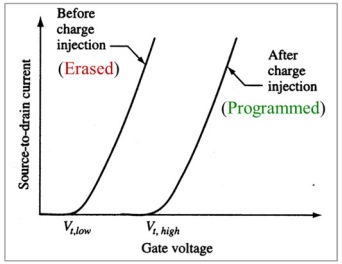
- For electron injection in an nMOSFET:
  - Charges stored → V_T shifts to $V_{t,high}$ → High-threshold state (高臨界狀態) → Programmed
  - Charges erased → V_T returns to $V_{t,low}$ → Low-threshold state (低臨界狀態) → Erased
- To read out the bit stored in the MOSFET, V_G is set between $V_{t,low}$ and $V_{t,high}$.



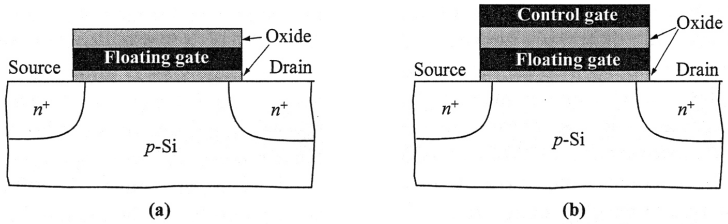
(a) Schematic diagram of a MOSFET nonvolatile memory device. (b) The MOSFET threshold voltage shifts from $V_{t,low}$ to $V_{t,high}$ after electron injection.

Programming & erasing times due to V_T transient (暫態)

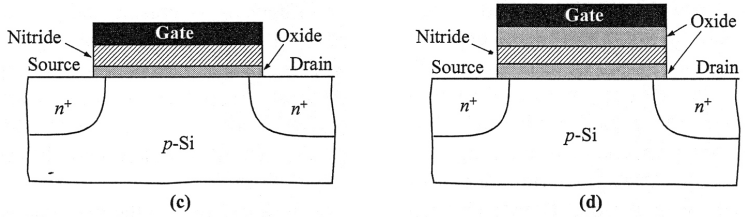




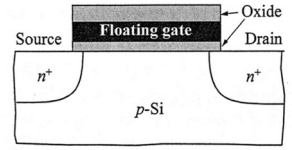
- **Floating-gate devices** (浮動閘極元件) :
  - (a) FAMOS (floating-gate avalanche-injection MOS).
  - (b) Stacked-gate transistor.



- **Charge-trapping devices** (電荷捕陷元件) :
  - (c) MNOS (metal-nitride-oxide-silicon) transistor.
  - (d) SONOS (silicon-oxide-nitride-oxide-silicon) transistor.



Floating-Gate NVM



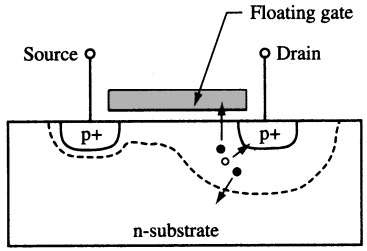
Floating-gate devices (浮動閘極元件) :

FAMOS (floating-gate avalanche-injection MOS).

(浮動閘極累增注入MOS)

Stacked-gate transistor.

- FAMOS is one of the earliest successful floating-gate memory products.
- It's typically a pMOSFET, because, for the FAMOS operation, the injection of hot electrons in a pMOSFET is much more efficient than that in an nMOSFET.
- Programming is by avalanche *hot electron injection*, while erasure is by UV light or X-ray as the device has no control gate.
- When the device is programmed, the electrons stored in the floating gate induce an inversion channel of holes, thus making the device conducting.

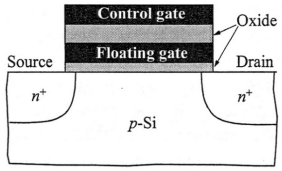


Schematic of a FAMOS device. The dotted line indicates the boundary of the depletion region.

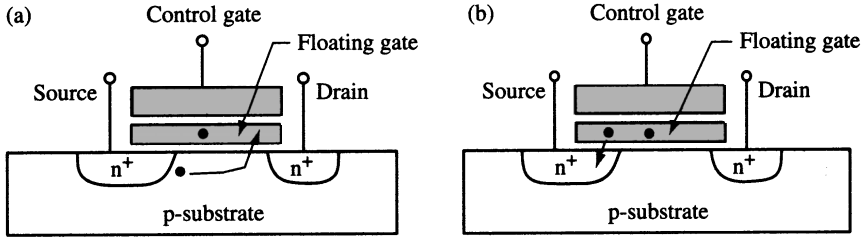
Floating-gate devices (浮動閘極元件) :

FAMOS (floating-gate avalanche-injection MOS).

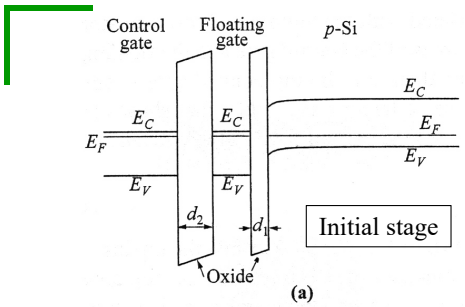
Stacked-gate transistor (堆疊閘極電晶體).

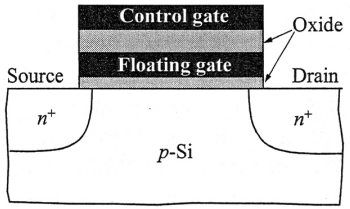


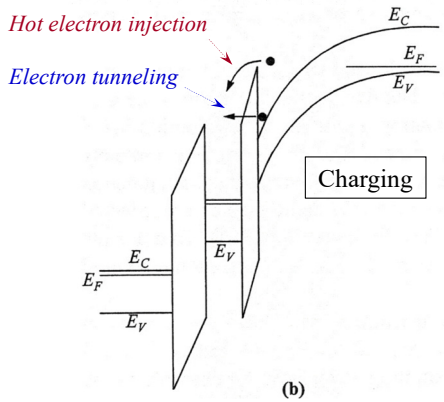
- There is a control gate.
- Programming is by *hot electron injection* or *electron tunneling* near the drain region, while erasure is by *electron tunneling* from the floating gate to the source region. (*Next pages for details*)

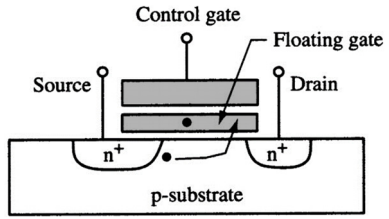


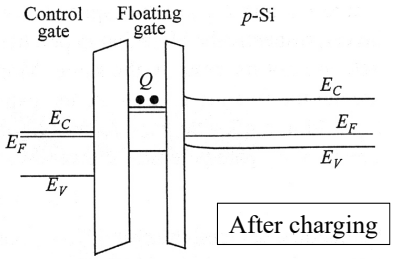
Schematic diagrams of a stacked-gate nonvolatile memory device. (a) Programming by channel hot electron injection. (b) Erasure by electron tunneling from floating gate to source.



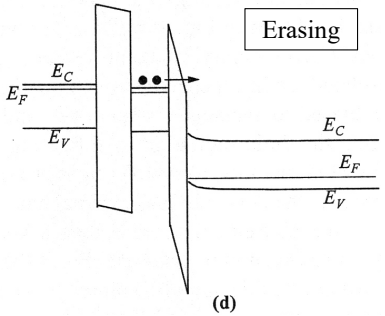




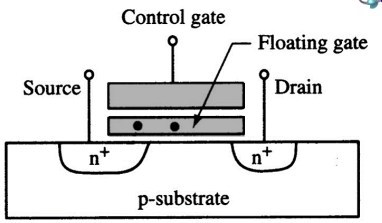


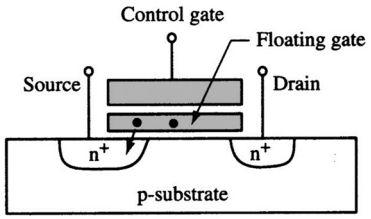


(c)

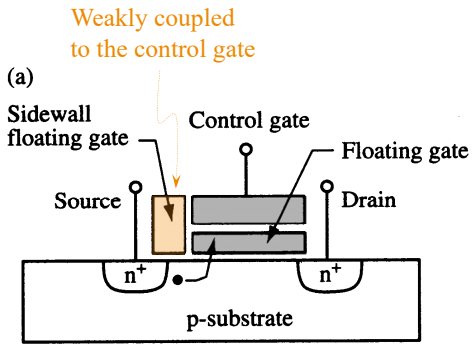


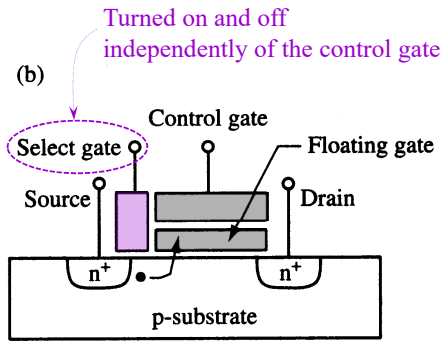
(d)





Two cases using source-side injection (源極側注入)

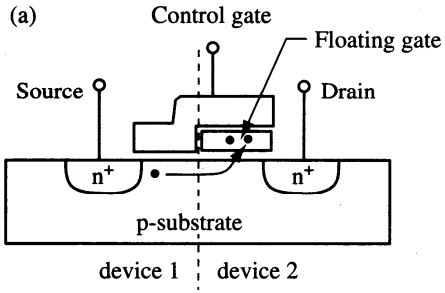




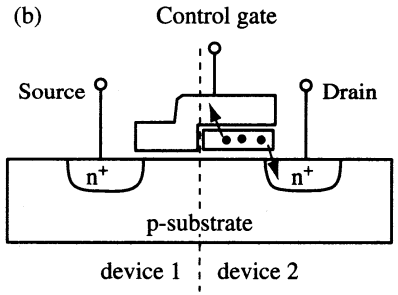
Schematics of floating-gate devices using source-side hot electron injection. (a) A stacked-gate device having a second floating gate at the source end. (b) A stacked-gate device having a second gate (select gate) at the source end.

Using a split control gate (分離控制閘極)

Programming



Erasing



Schematic diagrams of a stacked-gate nonvolatile memory device having a split control gate. (a) Programming by channel hot electron injection. (b) Erasure can be accomplished by tunneling electrons from the floating gate to the drain region or to the control gate.

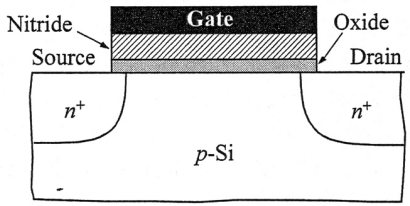
Charge-Trapping NVM

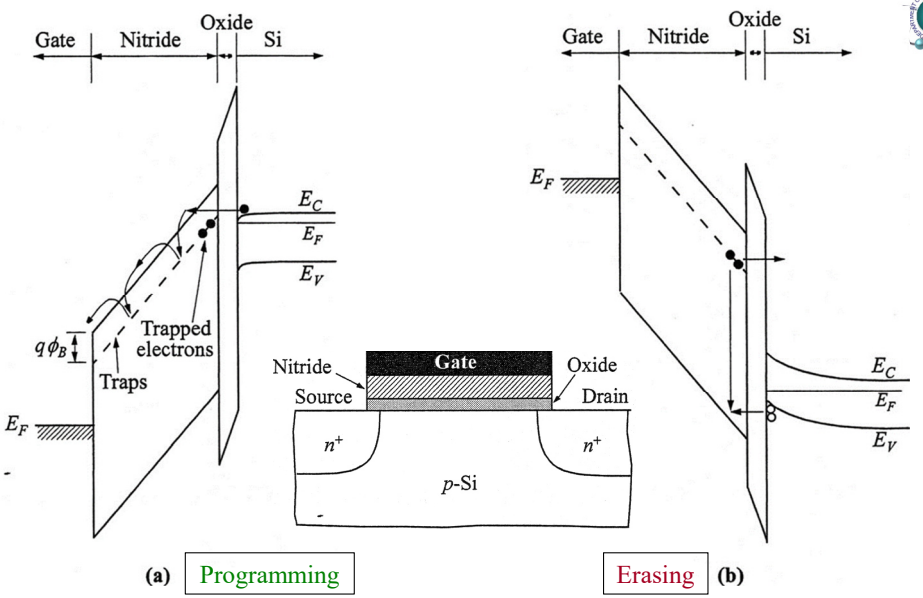
Charge-trapping devices (電荷捕陷元件) :

MNOS (metal-nitride-oxide-silicon) transistor.

SONOS (silicon-oxide-nitride-oxide-silicon) transistor.

- The simplest EEPROM devices based on charge storage in the gate insulator.
  - The silicon-nitride layer is used as an efficient material to trap electrons.
  - Electrons are trapped in the nitride layer close to the oxide-nitride interface.
- Programming and erasure are by electrons and/or holes tunneling into and out of the nitride layer, depending on whether the device is an nMOSFET or a pMOSFET.





Rewriting of MNOS memory. (a) Programming: electrons tunnel through oxide and are trapped in the nitride. (b) Erasing: holes tunnel through oxide to neutralize the trapped electrons, and tunneling of trapped electrons.

SONOS (silicon-oxide-nitride-oxide-silicon) transistor.

- Sometimes called MONOS (metal-oxide-nitride-oxide-silicon) transistor.
- The function of the top blocking layer is to prevent electron injection from the metal to the nitride layer during erase operation.