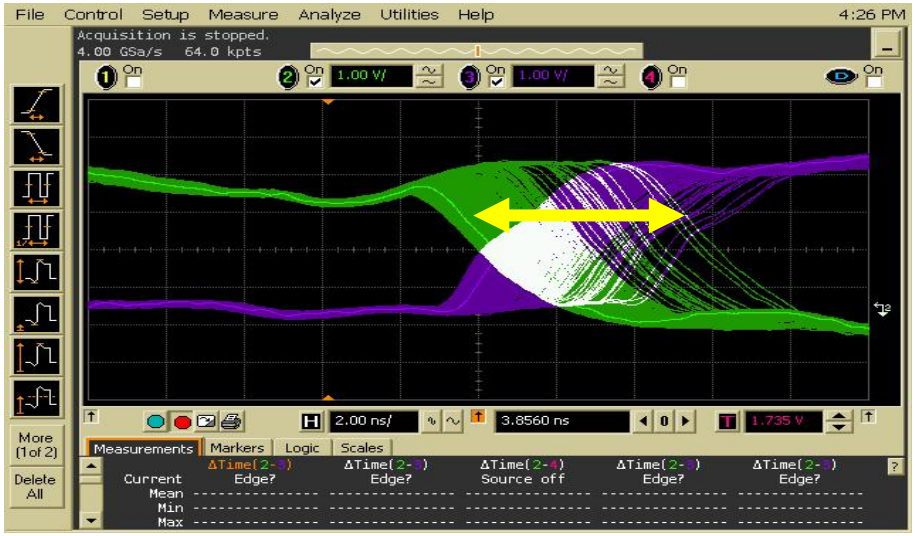
A Fully Synthesizable High-Precision Built-In Delay Time Measurement Circuit

Ching-Hwa Cheng

Dept. Electronic Engineering
Feng-Chia University Taiwan, R.O.C.

研究動機

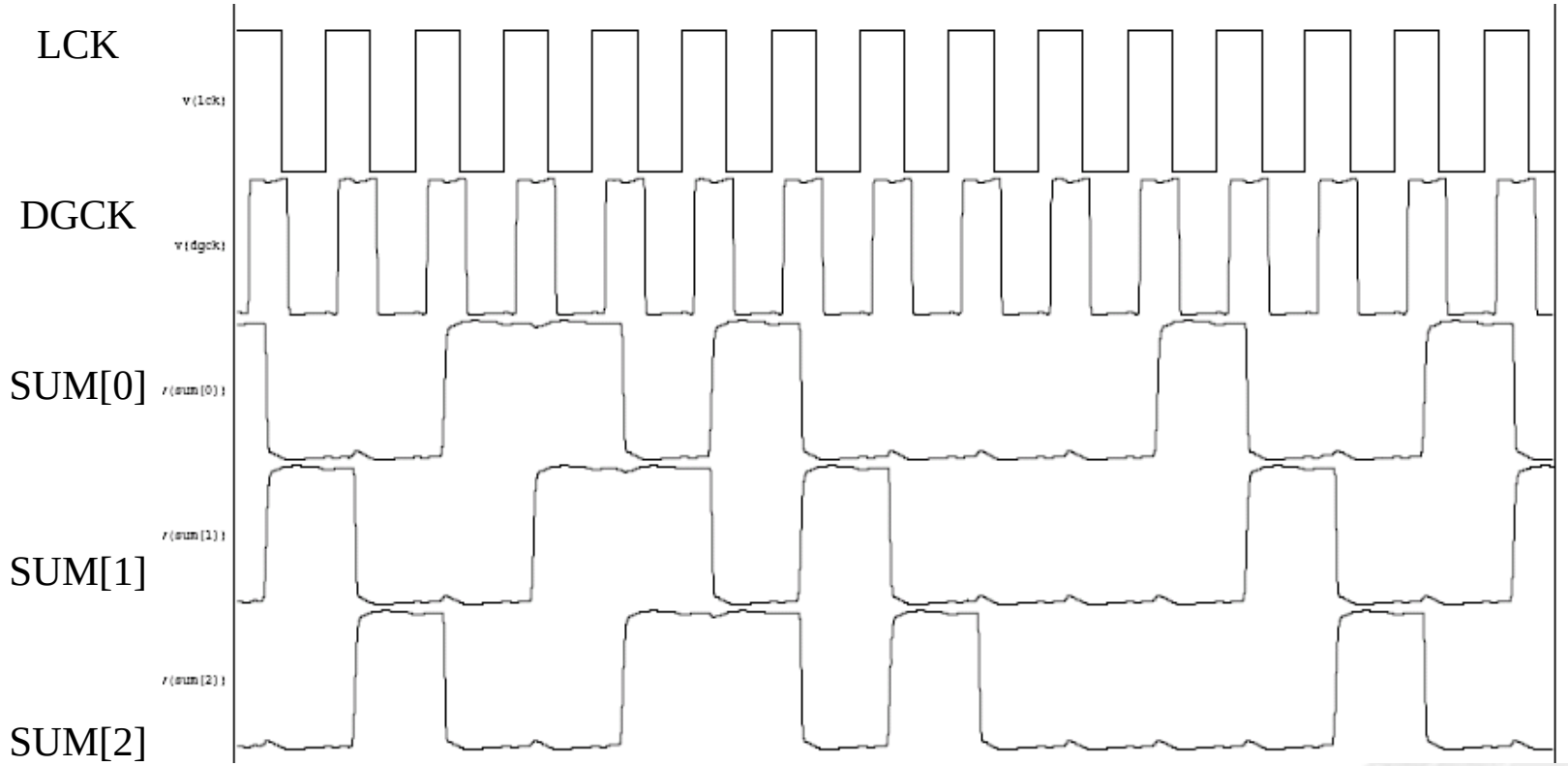

File Control Setup Measure Analyze Utilities Help 4:26 PM
Acquisition is stopped.
4.00 GSa/s 64.0 kpts
1.00 V/
2.00 ns/
3.8560 ns
1.735 V
Measurements Markers Logic Scales
More (1 of 2)
Delete All


File Control Setup Measure Analyze Utilities Help 4:38 PM
Acquisition is stopped.
4.00 GSa/s 64.0 kpts
1.00 V/
2.00 ns/
3.8560 ns
1.735 V
Measurements Markers Logic Scales
More (1 of 2)
Delete All

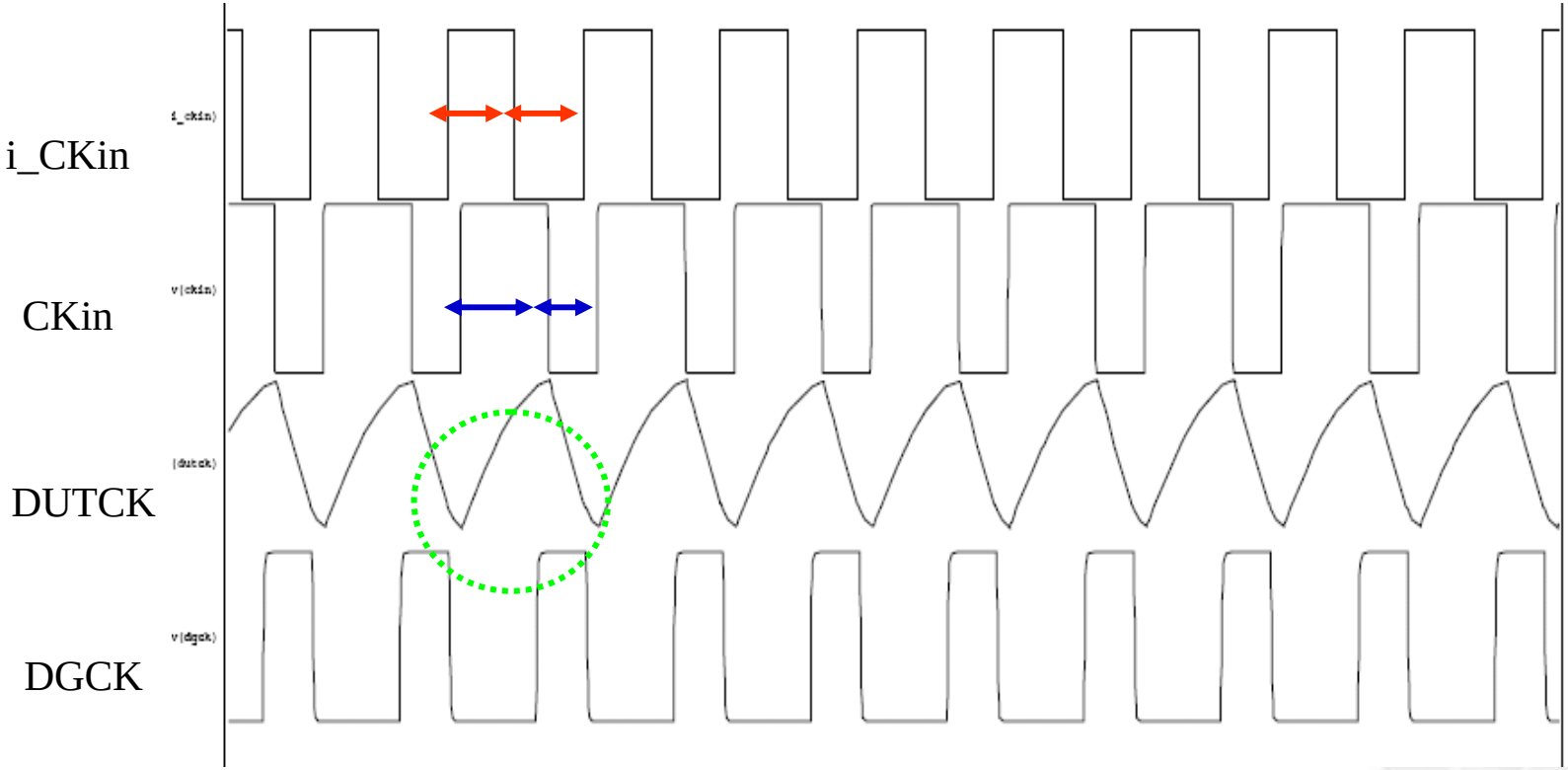

File Control Setup Measure Analyze Utilities Help 2:51 PM
Acquisition is stopped.
4.00 GSa/s 64.0 kpts
1.00 V/
2.00 ns/
65.1720 ns
1.650 V
Scales
Source channel 1
Vertical Scale 1.00 V/div
Offset 1.481 V
Horizontal Scale 2.00000 ns/div
Position 65.1720 ns
More (1 of 2)
Delete All


File Control Setup Measure Analyze Utilities Help 2:52 PM
Acquisition is stopped.
4.00 GSa/s 64.0 kpts
1.00 V/
2.00 ns/
65.1720 ns
1.650 V
Scales
Source channel 1
Vertical Scale 1.00 V/div
Offset 1.481 V
Horizontal Scale 2.00000 ns/div
Position 65.1720 ns
More (1 of 2)
Delete All

Clock Signal Postsim



Clock PostLayout Simulation Waveforms

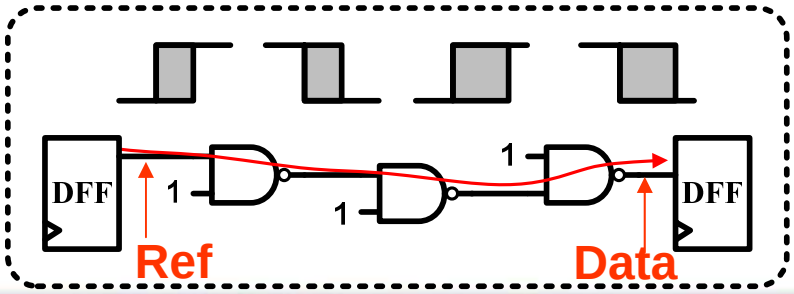


Outline

- Introduction
- The Built-in Delay Measurement (BIDM) Circuit Design
- Different Circuit Structure Comparisons
- The BIDM Circuit Simulations
- Chip Validation
- Extended BIDM Design
- Conclusions
- Reference

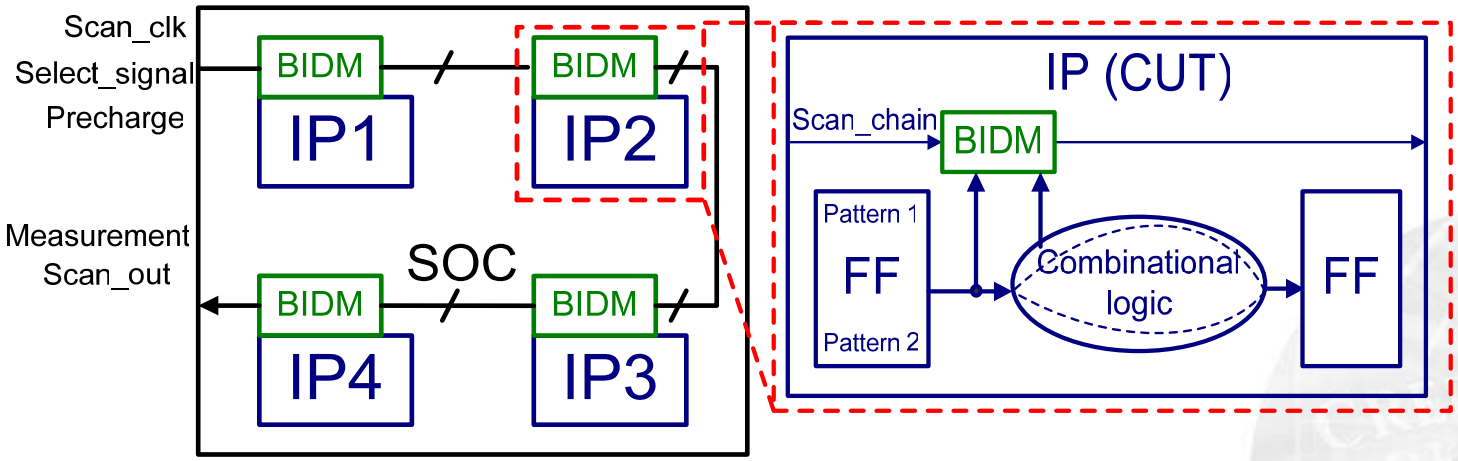
Introduction

- Delay testing has become a major issue for manufacturing advanced System on a Chip.
- The Circuits Under Test (CUT) have many circuit paths and dependent input patterns; it is hard to measure delay times accurately, especially when debugging small delay defects.
- A segment delay defect on a path can be observed by propagating a transition through the path.



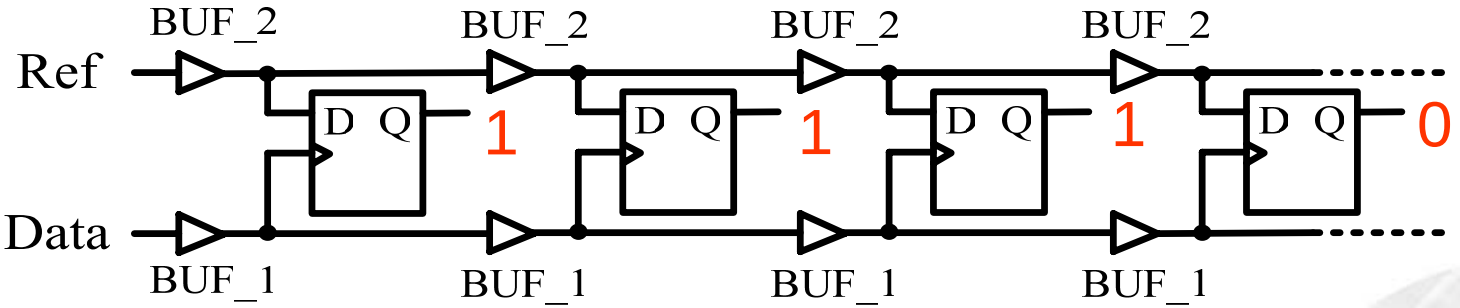
Introduction

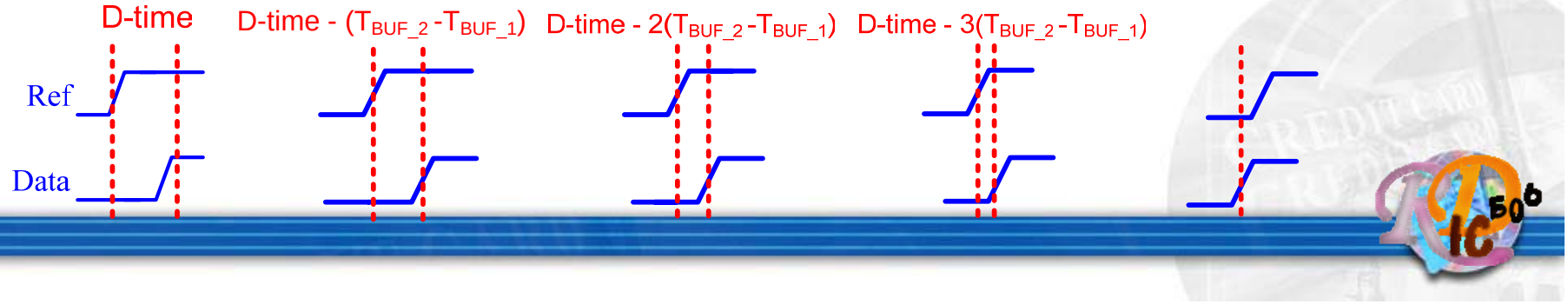
- We propose a fully synthesizable high resolution built-in delay measurement (BIDM) circuit that applies vernier delay line (VDL).
- The focus of our BIDM is to accurately measure delay time for internal chip debugging.



The Vernier Delay Line Circuit

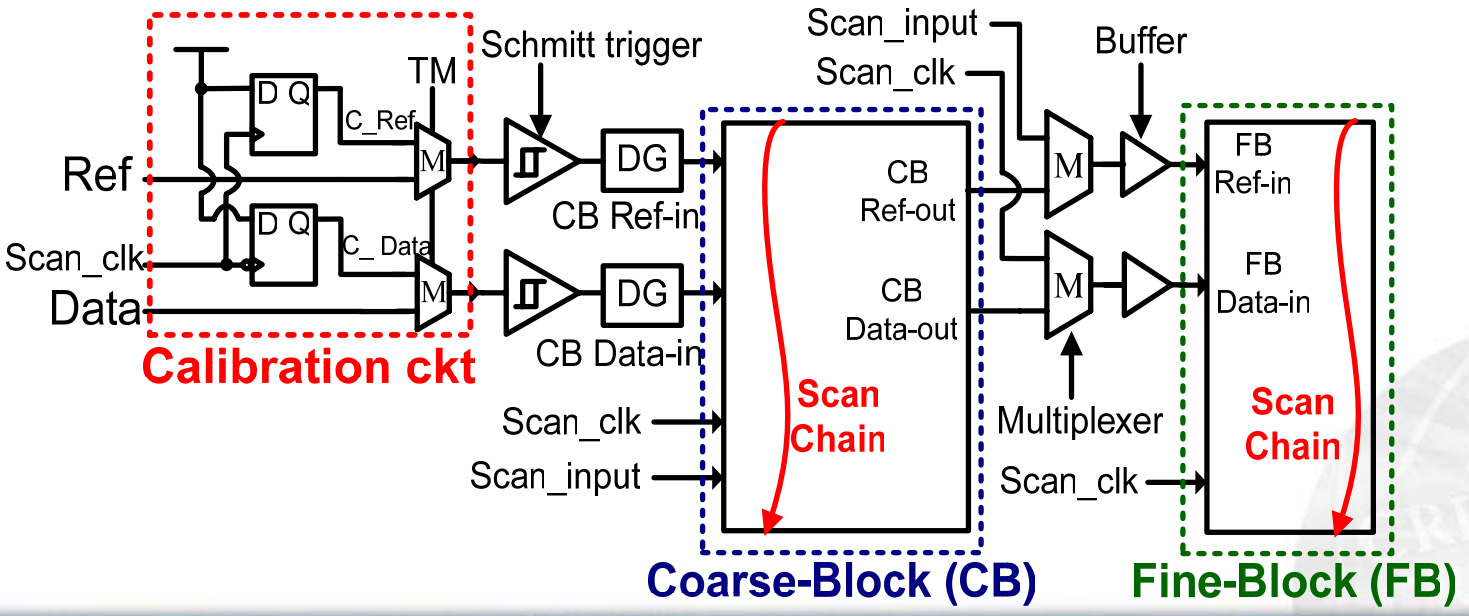
- Vernier delay line (VDL)
  - Each stage of a VDL is constructed by a positive edge trigger D-type Flip-Flops and two buffers, and BUF_2's delay time is larger the BUF_1's.
  - The VDL circuit transforms the two signals' D-time into digital format, which can be recorded into DFF.





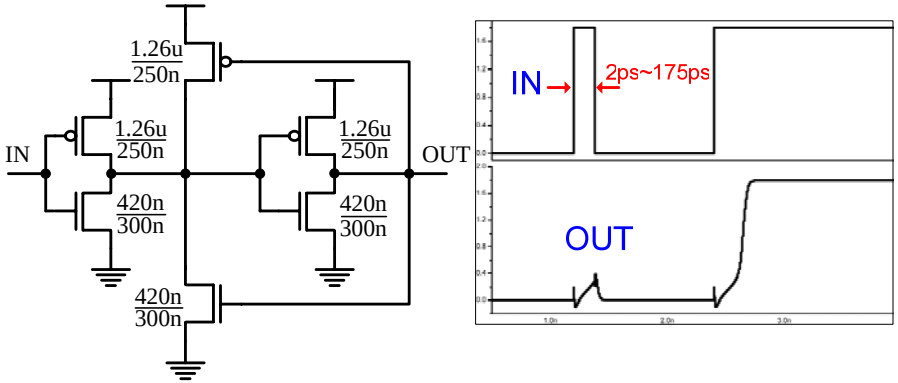
The BIDM Circuit Design

- The BIDM's architecture is divided into two main block, namely Coarse-Block (CB) and Fine-Block (FB).
- The FB's resolution is smaller than CB's resolution. Our design concept is similar to the ten's digital system: FB uses 2 tens digits, CB uses 3 tens digits.

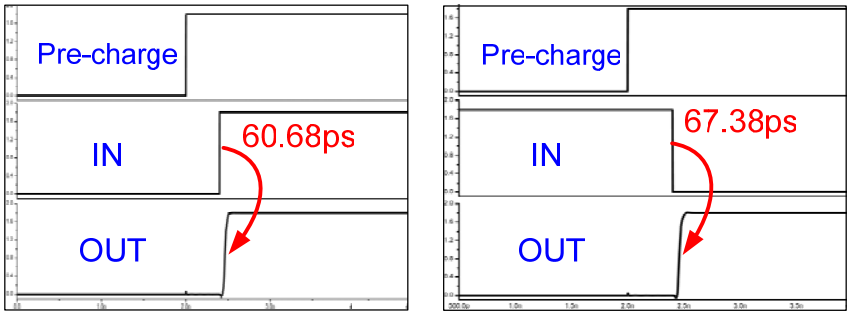


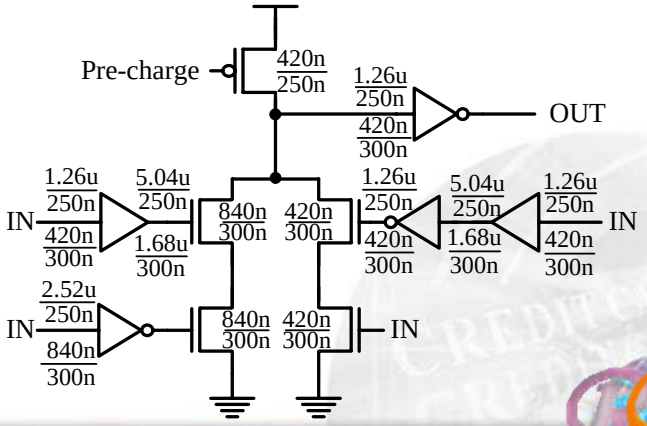
The BIDM Circuit Design

- Schmitt Trigger
  - The two signals (Ref and Data) pass a schmitt trigger to diminish glitches (2~175ps).



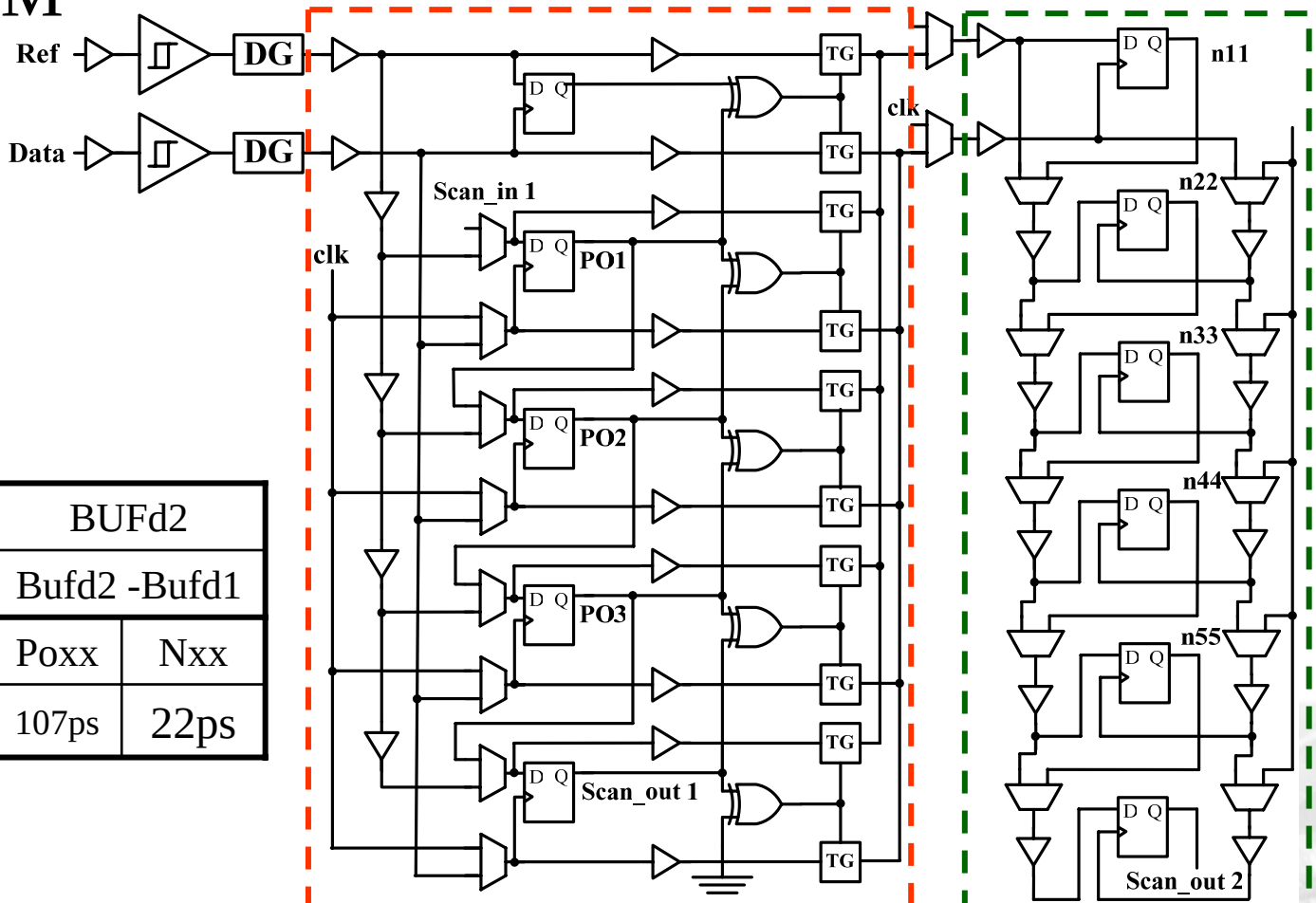
- Dynamic Gate (DG)
  - The two input signals (Ref and Data) have four type transitions. The DG circuit can be used to transfer the Ref and Data signals to rise-transition.





The Detail Circuit Structures

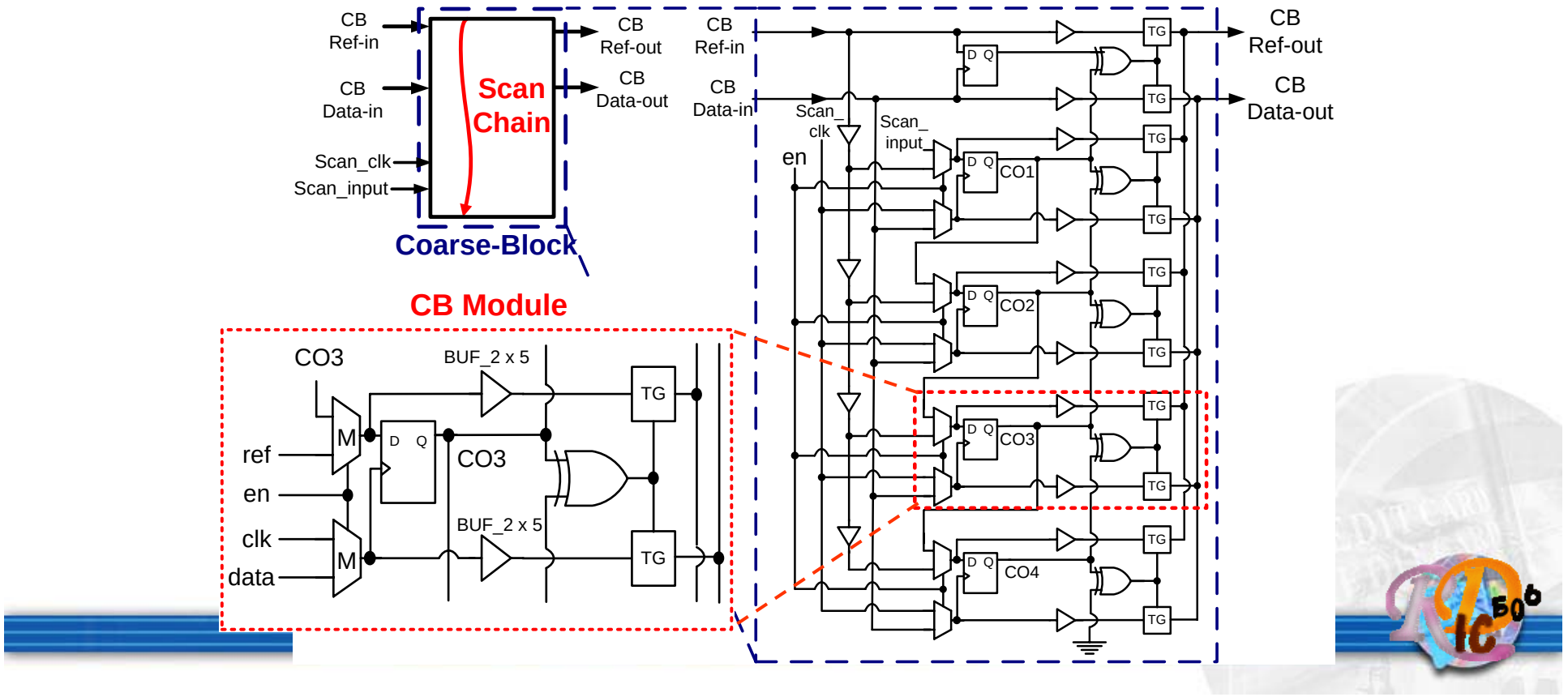
- BIDM



Poxx	BUFd2	
nxx	Bufd2 -Bufd1	
	Poxx	Nxx
Avg Range	107ps	22ps

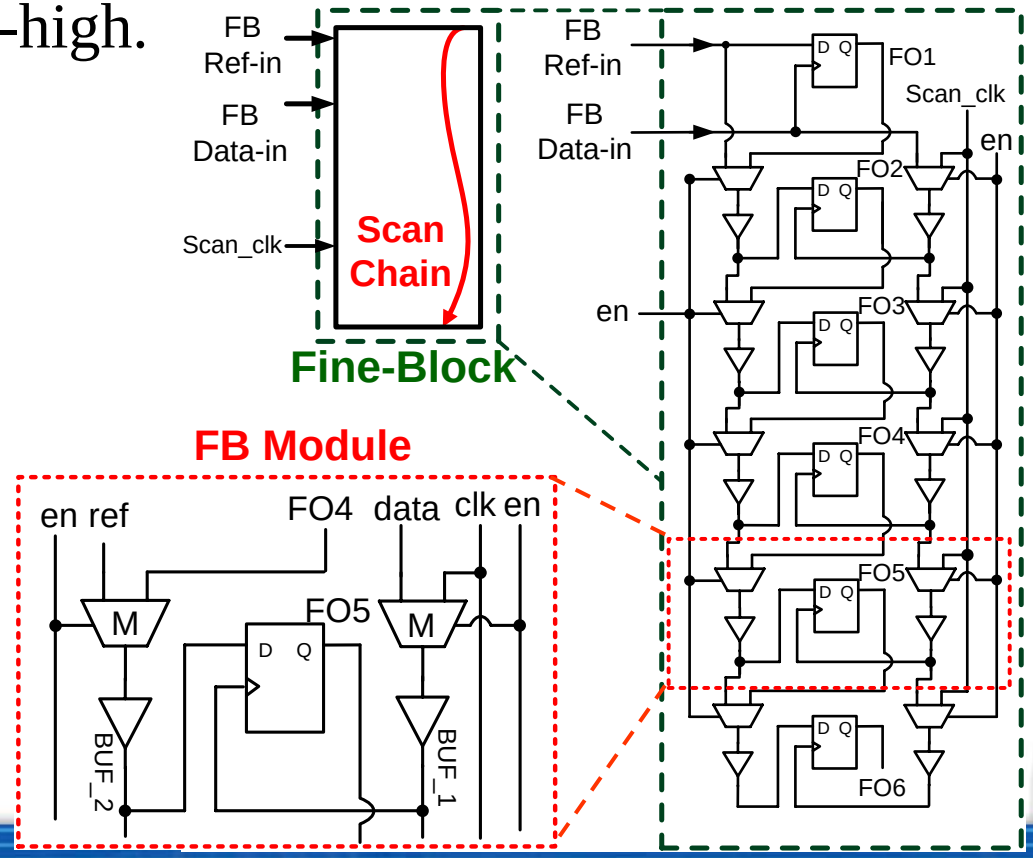
The BIDM Circuit Design

- The Coarse Block Circuit Design
  - The average D-time range is 130ps for CB outputs.
  - The TGs are used to decide whether the Ref and Data signals need to pass into the FB or not.



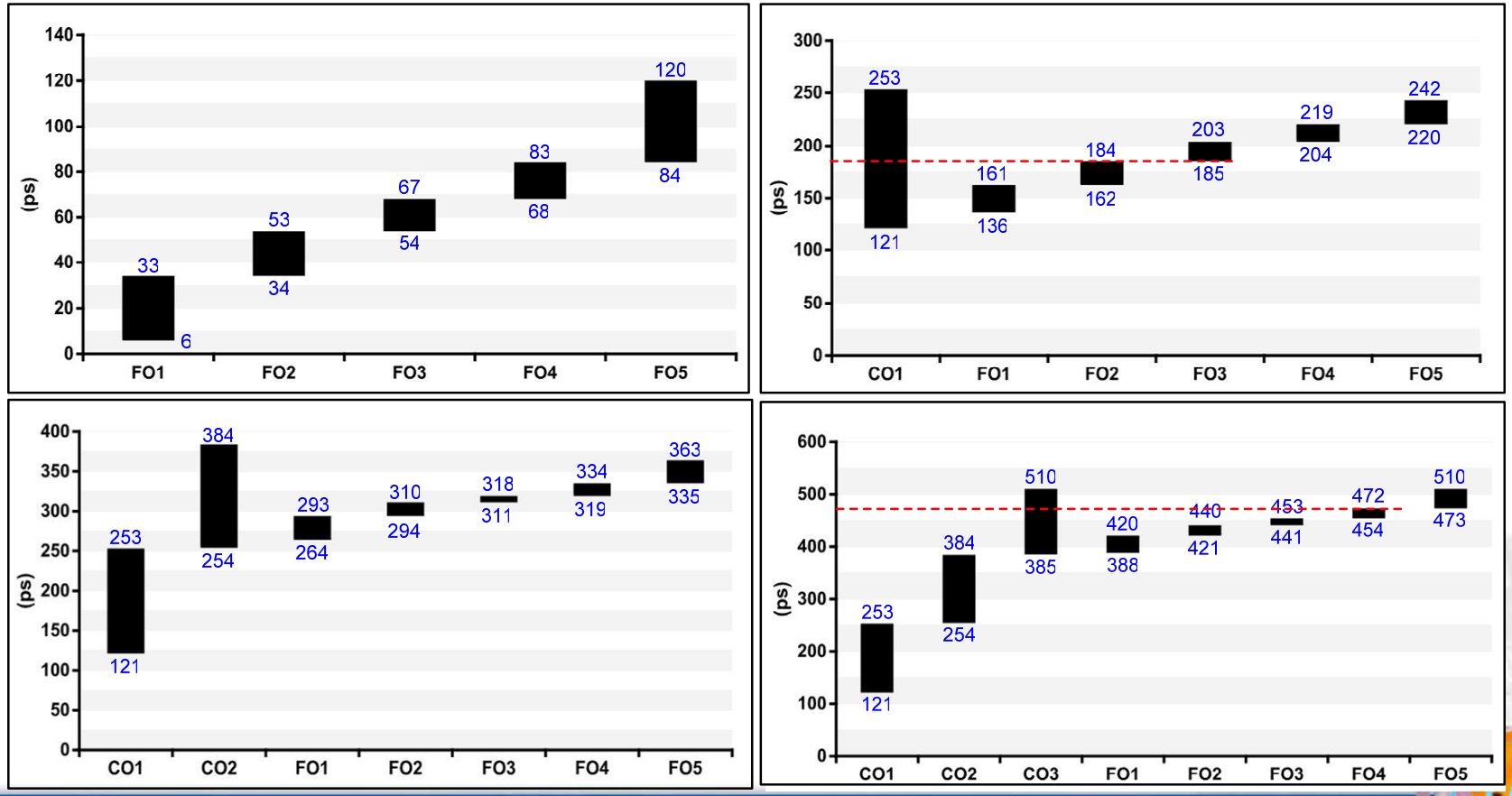
The BIDM Circuit Design

- The Fine Block Circuit Design
  - The average D-time range is 21.35ps for FB outputs.
  - When the D-time increases, more FB outputs will be logic-high.



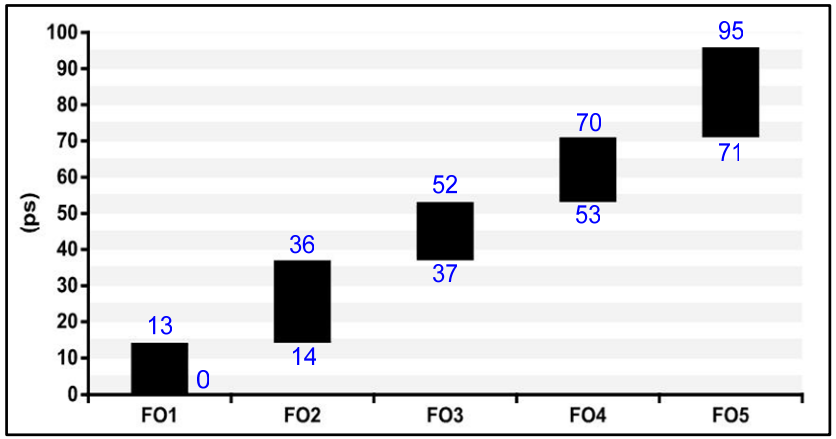
BIDM Circuit Simulation

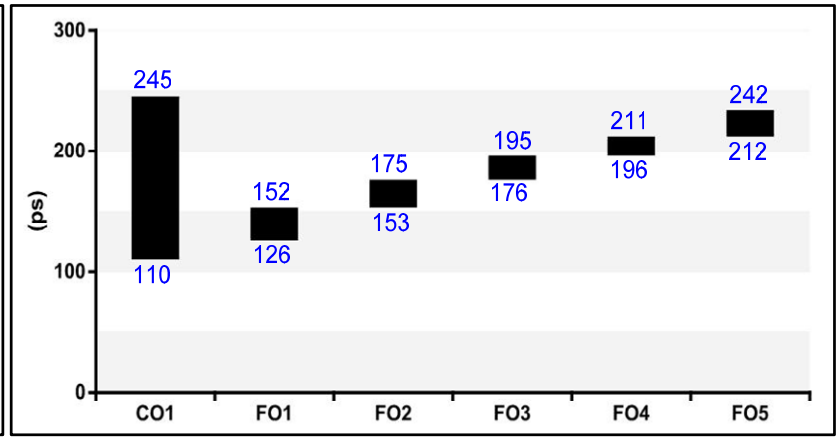
- The timing measurement range
  - Rise/Rise Signals

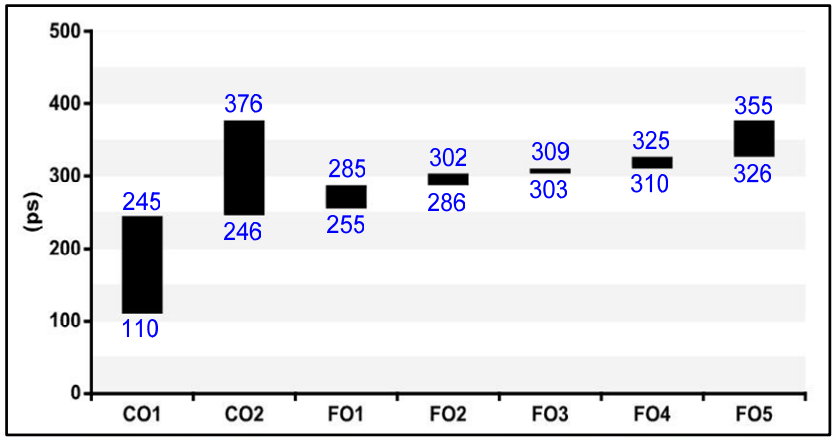


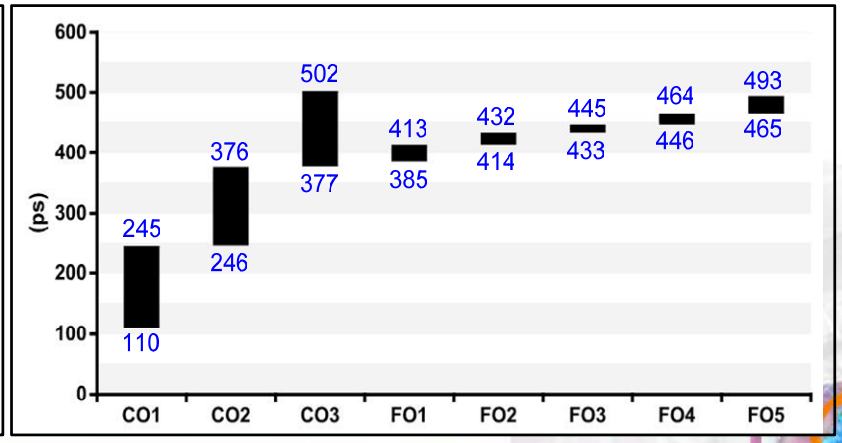
BIDM Circuit Simulation

- The timing measurement range
  - Rise/Fall Signals







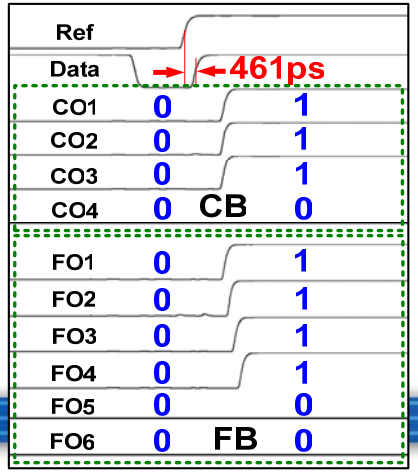


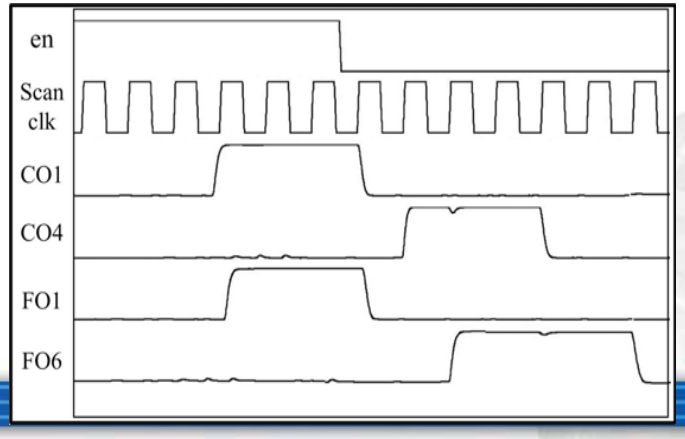
BIDM Circuit Simulation

- The CB and FB average measurement results.

Time range		6~120ps	121~253ps	254~384ps	385~510ps	Average
Rise Rise	CO		133±2.9ps	131±2.9ps	126±2.9ps	130ps
	FO	19±5.4ps	21.4±3.5ps	20±8.4ps	25±9.4ps	21.35ps
Time range		**0~109ps**	**110~245ps**	**246~376ps**	**377~502ps**	**Average**
Rise Fall	CO		136±4.1ps	131±4.1ps	126±4.1ps	131ps
	FO	19.2±4.2ps	21.6±3.6ps	20.2±9.1ps	21.8±6.3ps	20.7ps

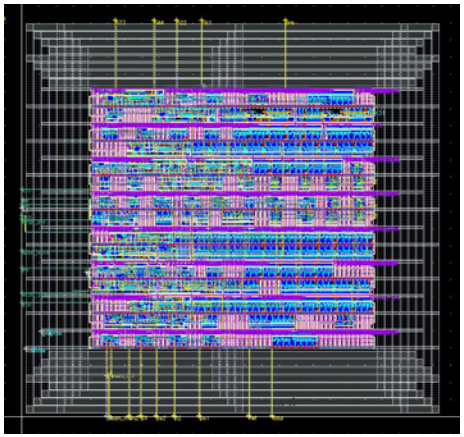
- The integrated circuit of CUT with BIDM post-layout simulation.
  - The D-time range is 454~472ps in simulation result. The BIDM report D-time range covers a real delay time of 461ps.

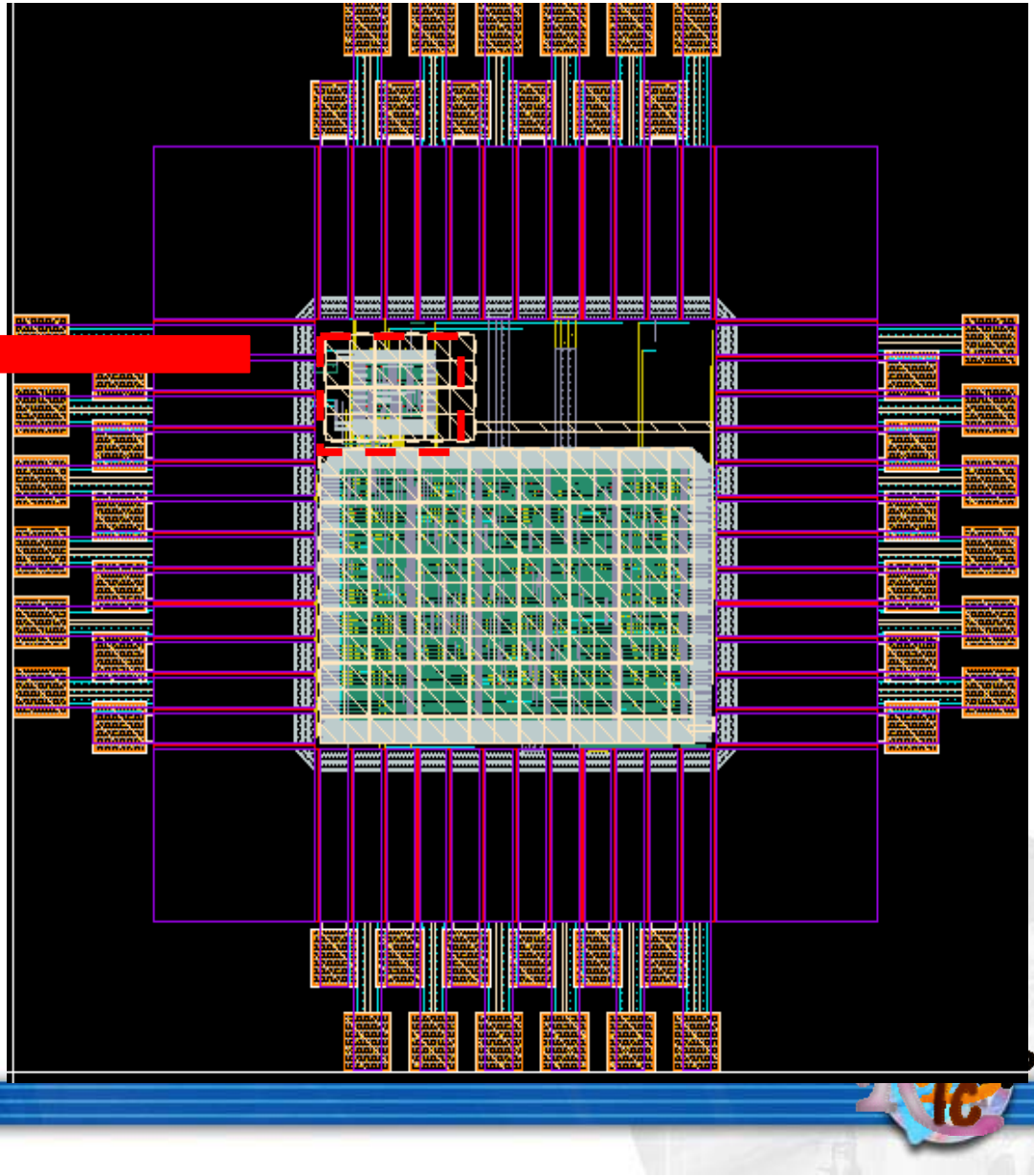




Layout Photo View

BIDM

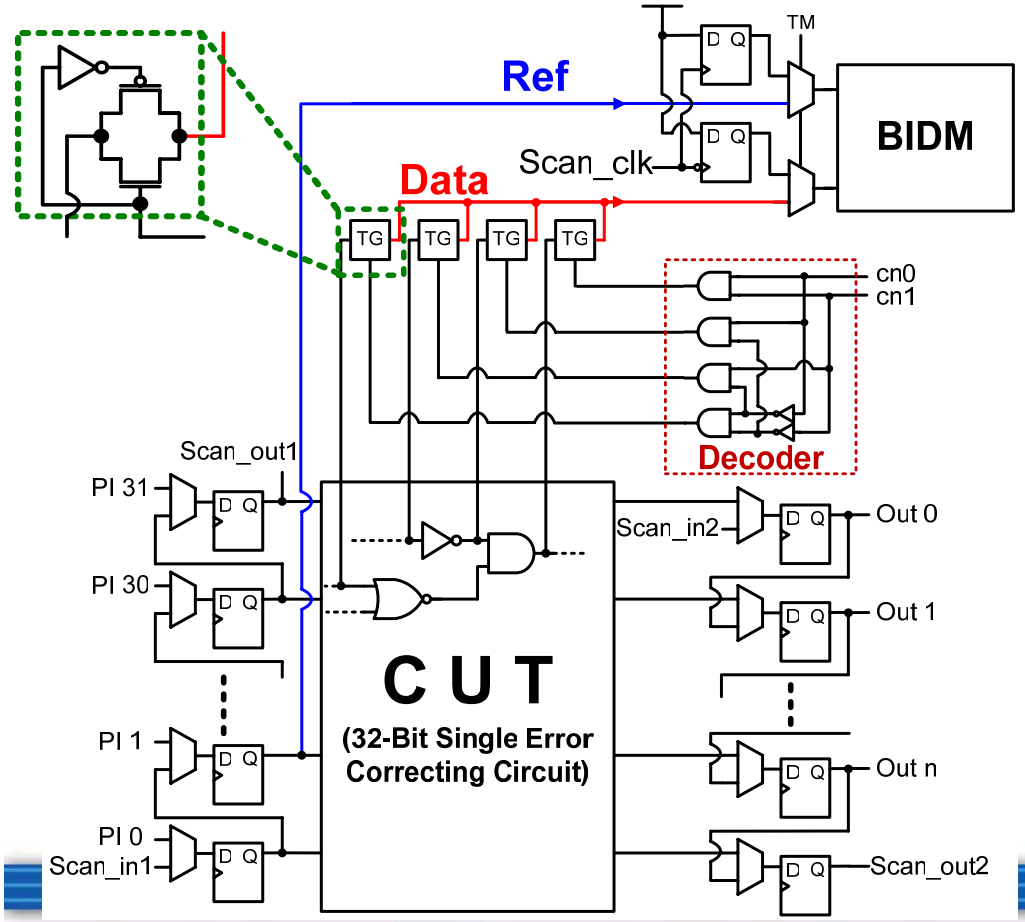


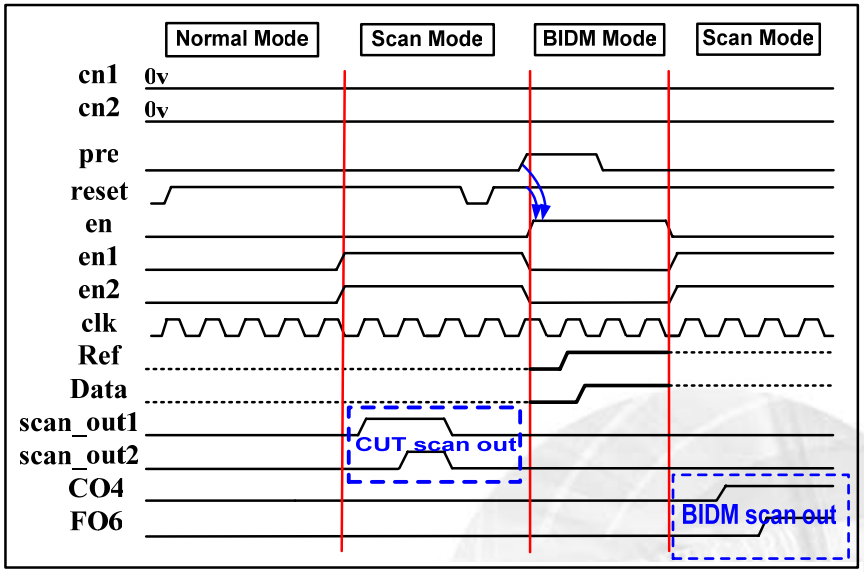


Circuit	Design an EMI Tolerant Built-In Delay Self Testing Circuit
Process	TSMC 1P6M 0.18um
Package	48 S/B (Package type)
Chip area	1.472*1.465 mm^2
Transistor count	7938
Max. Power	5216.0517uW

Test Circuit Implementation

- The integrated circuit of CUT with BIDM
  - The integrated test chip was implemented by a cell-based design flow using TSMC 0.18um technology.





The test application control timing diagrams

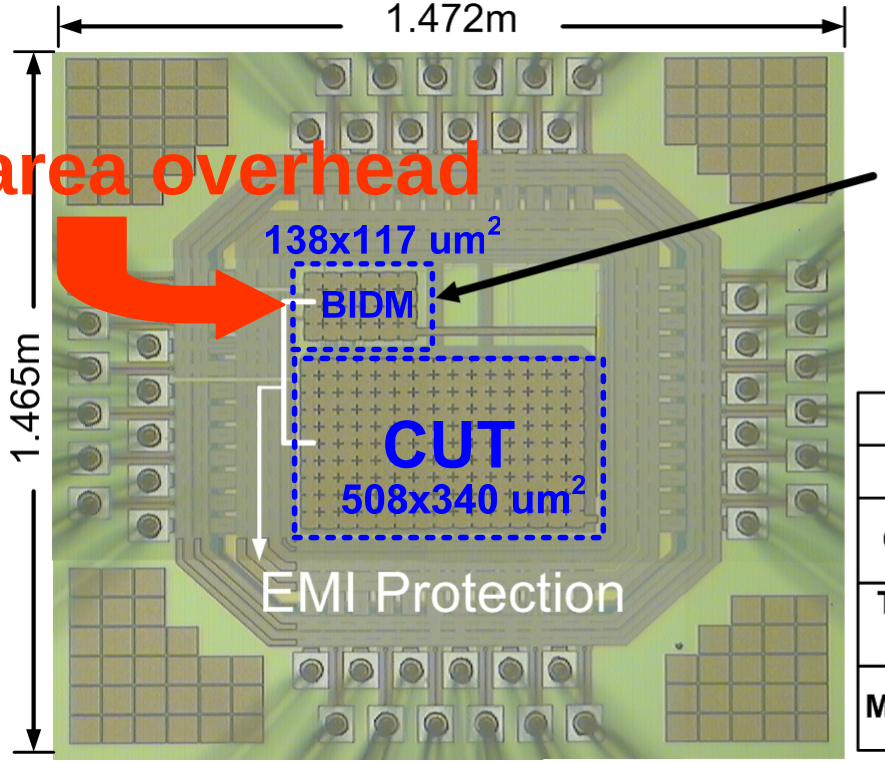
Test Circuit Postlayout Simulation

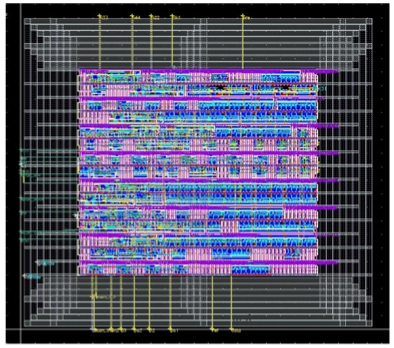
- The integration circuit corner simulation results based on the **TT**, **FF**, and **SS** TSMC 0.18um SPICE Model.
  - The *Nanosim* SPICE simulator is used in this integrated circuit simulation.
  - The SS model simulation results indicate failure, and the measurement results cannot be adopted.

Case/Tr Model	Case1			Case2			Case3			Case4		
	FF	TT	SS	FF	TT	SS	FF	TT	SS	FF	TT	SS
Ref (ps)	11711	**11891**	Fail	11712	**11885**	Fail	11712	**11885**	0	11711	**11885**	Fail
Data (ps)	11662	**11849**	12279	11837	**12063**	12551	11843	**12066**	12583	12068	**12346**	Fail
D-time (ps)	-49	**-42**	w/o	125	**178**	w/o	131	**181**	w/o	357	**461**	w/o

Chip Validation

- The die photo
  - To Electric Magnetic Interference (EMI) noise from adversely impacting the BIDM.

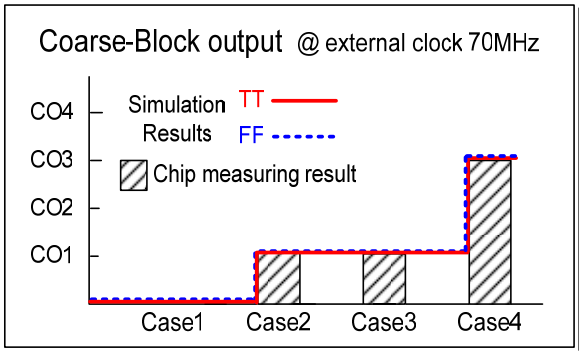


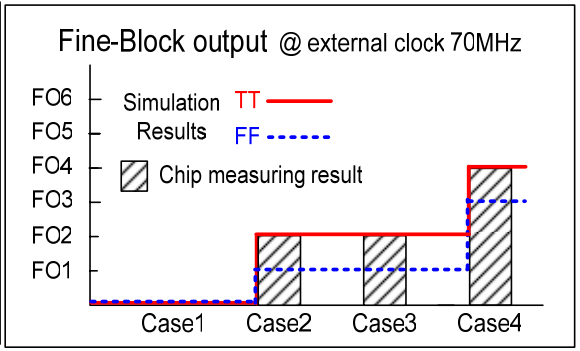


Process	TSMC 1P6M 0.18um
Package	48 S/B
Chip area	1.472x1.465 mm^2 BIDM: 1.38x117 um^2
Transistor count	7938 BIDM: 1118
Max. Power	5.216mW BIDM: 1.807mW

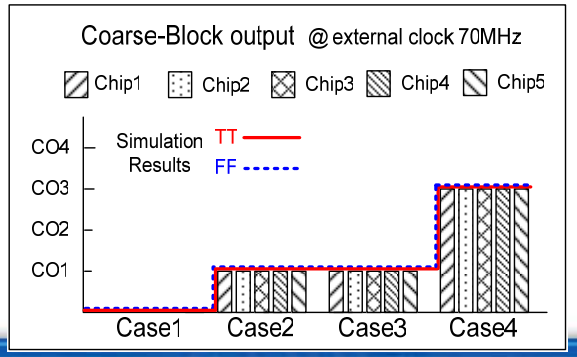
Single Chip Validation Results

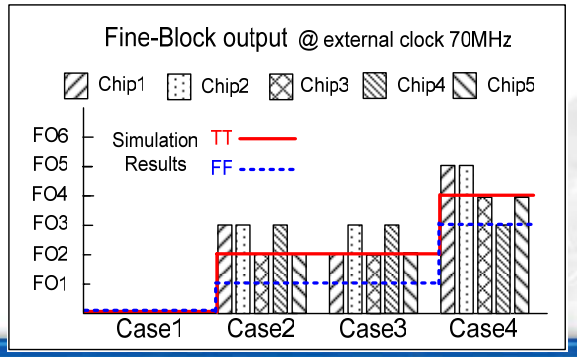
- Chip measuring result of Case1 to Case4
  - We take the TT model simulations as our reference in the analysis.
  - The chip measurement results are the same as those of the TT model.





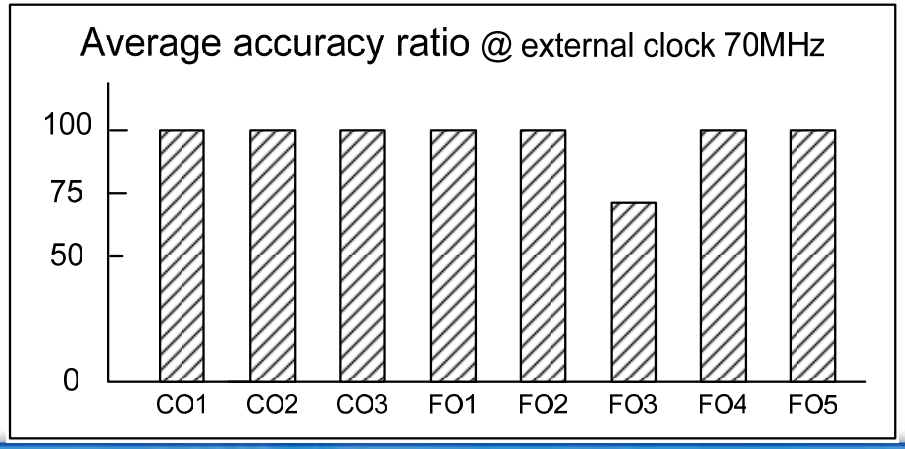
- The measuring result from five chips





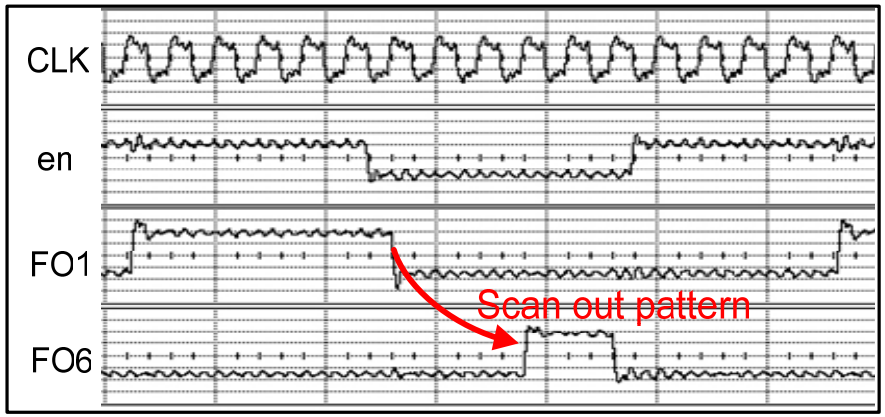
Single Chip Validation Results

- The average accuracy ratio from all test cases.
  - We monitored 14 other test cases by changing the input patterns for Chip-3.
  - The BIDM can accurately report the node D-time, and (except for FO3 and FO5) most of the outputs correctly match the simulation results.
  - The average accuracy ratio is 95.83% for total 18 test cases.

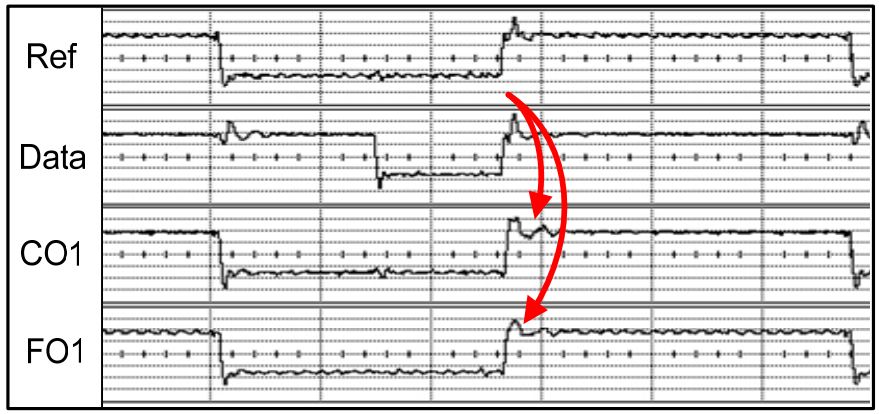


Oscillator Scope Measurements

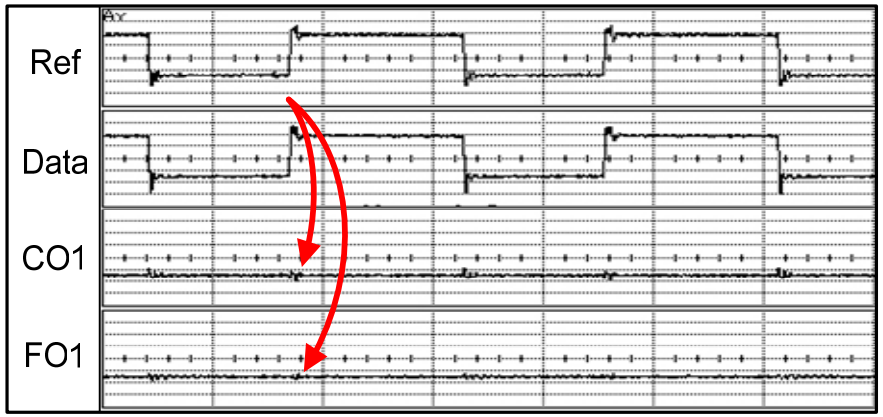
- The scope measurement waveforms of chip



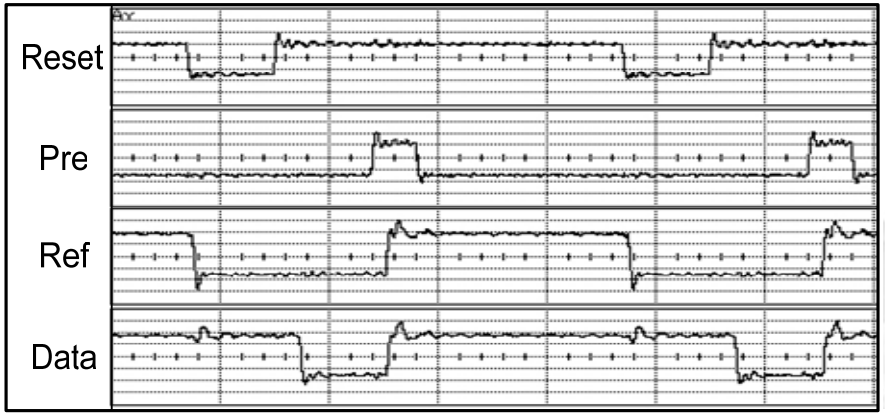
(a) The correct scan the FO1 output to FO6 stage.



(b) The CO1 and FO1 correct response the D-time.



(c) No response in CO and FO, when D-time<0



(d) The BIDM chip control signals timing diagram.

Conclusions

- Our BIDM is digitally designed; it can be easily synthesized within a CUT with little area overhead.
- The BIDM can accurately measure the small path delay time from an internal chip, and report the timing measurement results to outside observation by scan chains.
- Our BIDM improve the timing resolution capability of shorter path delay to make the internal segment path delay measurement/test practice.

Reference

[1] X. Lin, R. Press, J. Rajski, P. Recuter, T. Rinderknecht, B. Swanson, N. Tamarapalli, “High-Frequency At-Speed Scan Testing”, IEEE Design & Test of Computers, pp. 17-25, 2003.

[2] M. J. Hsiao, J. R. Huang, T. Y. Chang; “A Built-in Parametric Timing Measurement Unit”, IEEE Design & Test of Computers, Vol. 21, pp. 322-330, 2004.

[3] R. Datta, A. Sebastine, J. A. Abraham, “Delay fault testing and silicon debug using scan chains”, IEEE European Test Symposium, pp. 46 – 51, 2004.

[4] R. Datta, A. Sebastine, A. Raghunathan, J. A. Abraham. “On-chip Delay Measurement for Silicon Debug,” IEEE Great Lakes Symposium on VLSI, pp.145-148, 2004.

[5] A. Raychowdhury, S. Ghosh, K. Roy, “ A Novel On-Chip Delay Measurement Hardware for Efficient Speed-Binning,“ IEEE International On-Line Testing Symposium, pp.287-292, 2005.

[6] A. Raychowdhury, S. Ghosh, S. Bhunia, D. Ghosh, K. Roy, “A Novel Delay Fault Testing Methodology Using On-Chip Low-Overhead Delay Measurement Hardware at Strategic Probe Points,” IEEE European Test Symposium, pp. 108-113, 2005.

[7] S. Ghosh, S. Bhunia, A. Raychowdhury, K. Roy, "Delay Fault Localization in Test-Per-Scan BIST Using Built-In Delay Sensor," IEEE International On-Line Testing Symposium, pp. 31-36, 2006.

Reference

[8] R. Datta, R. Gupta, A. Sebastine, J.A. Abraham, “Tri-Scan : A Novel DFT Technique for CMOS Path Delay Fault Testing,“ IEEE International Test Symposium, pp. 1118-1127, 2004.

[9] R. Datta, G. Carpenter, K. Nowka, J.A. Abraham, “A Scheme for On-chip Characterization,” IEEE VLSI Test Symposium, pp. 24-29, 2006.

[10] K. Sung, L. S. Kim, **“**A high-resolution synchronous mirror delay using successive approximation register**”**, IEEE Journal Solid-State Circuits, Volume 39, Issue 11, pp. 1997 – 2004, Nov. 2004.

[11] K. T. Cheng, “Transition fault testing for sequential circuits”, IEEE Transactions on Computer-Aided Design of integrated Circuits and Systems, Volume 12, Issue 12, pp. 1971-1983, Dec. 1993

[12] Poki Chen, Chun-Chi Chen, Jia-Chi Zheng and You-Sheng Shen, “A PVT Insensitive Vernier-Based Time-to-Digital Converter with Extended Input Range and High Accuracy,” IEEE Transaction on Nuclear Science, vol. 54, pp. 294-302, Apr 2007.

[13] Rivoir, J., “Fully-Digital Time-To-Digital Converter for ATE with Autonomous Calibration”, IEEE International Test Conference, Santa Clara, CA, Oct. 2006

[14] P. Dudek, S. Szczpanksi, and J. V. Hatfield, "A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line," IEEE Trans. on Solid-State Circuits, vol. 35, no. 2, pp. 240-247, 2000.